DATA SHEET

SDN8080G
80-outputs common/segment driver

data sheet (v7) 2006 Apr 04

1 GENERAL

1.1 Description

The SDN8080G is a COMMON/SEGMEMT driver for large-panel dot-matrix STN LCD module. It can be used either as a COMMON driver or as a SEGMENT driver, by connecting its CS input to VDD or VSS.

When its CS input is connected to VDD, the SDN8080G is an 80-COMMON driver. When its CS input is connected to VSS, the SDN8080G is an 80-SEGMENT driver.

1.2 Features

- Operating voltage range (VDD-VSS, control logic): 2.7 ~ 5.5 volts.
- LCD bias voltage range (VDD-VEE): 6 ~ 28 volts.
- 80-SEGMENT driver or 80-COMMON driver, via CS-pin selection.
- When used as a SEGMENT driver, 4-bit parallel or 1-bit serial interface with a controller.
- When used as a COMMON driver, two modes of operation are available: Single mode or Dual mode.
- Display duty cycle: 1/64 ~ 1/256.
- LCD on/off control, when used as SEGMENT driver.
- External 4-level LCD bias voltage.
- Operating frequency range: 8 MHz, when VDD= 5 volts.
- Operating temperature range: -30 to +85 °C.
- Storage temperature range: -55 to +150 °C.

2 ORDERING INFORMATION

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SDN8080G-LQFPG	LQFP100 Pb-free package.
SDN8080G-QFPG	QFP100 Pb-free package.
SDN8080G-LQFP	LQFP100 general package.
SDN8080G-QFP	QFP100 general package.
SDN8080G-D	Tested die.

3 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

3.1 Functional block diagram

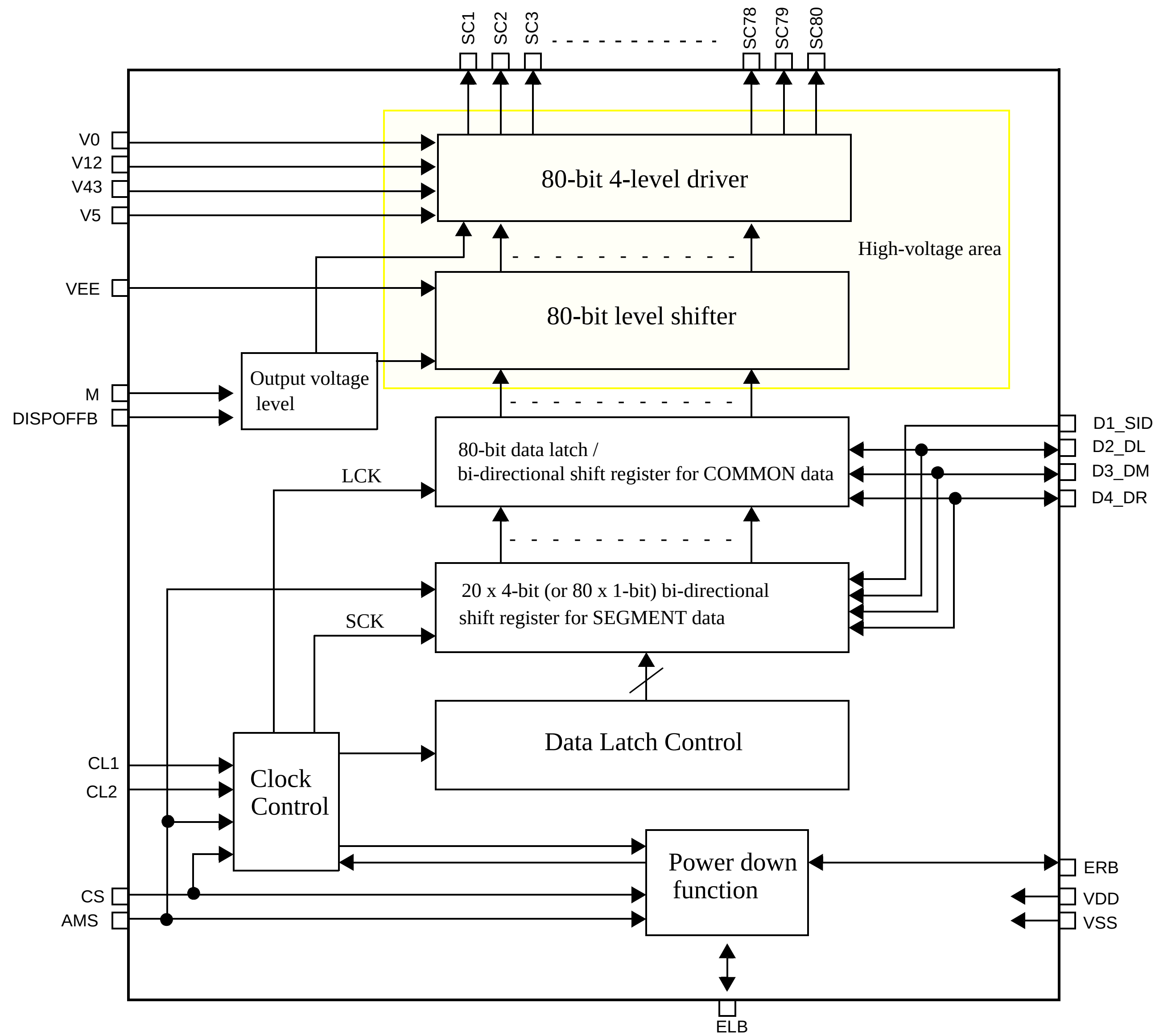


Fig.1 Functional diagram

3.2 Block description

Table 2 Block description

NAME	COM/SEG	DESCRIPTION
Clock control	COM/SEG	Inputs to this block are external signals CL1, CL2, CS, and AMS. It generates latch clock (LCK) and shift clock (SCK). SCK is used to shift display data into the 20 x 4-bit bi-directional shift register for SEGMENT data.
Data latch control	SEG	This block controls shift direction of the 20 x 4-bit shift register and selects its input data pins. In COMMON driver application, this block is disabled.
Power down function	SEG	This block enables or disables Clock Control block according to ERB/ELB input.
Output level selector	COM/SEG	Controls the output voltage level according to input signals M and DISPOFFB.
20 x 4-bit bi-directional shift register for SEGMENT data	SEG	This is the bi-directional 20 x 4-bit (80-bits) shift register for SEGMEMT data. In 1-bit serial interface mode of SEGMEN driver application, 80 SCK clocks are needed to shift in 80-bit data. In 4-bit parallel interface mode, only 20 SCK clocks are needed to shift in 80-bit data. In COMMON driver application, this block is disabled.
80-bit data latch, or bi-directional shift register for COMMON data	COM/SEG	In SEGMENT driver application, this block is used as an 80-bit data latch and the 80-bit data of the SEGMENT driver are latched into this latch for output. In single type COMMON driver application, this block is used as an 80-bit shift register. Depending on the value of SHL, 1-bit serial data is shifted into D2_DL or D4_DR. In dual type COMMON driver application, depending on the value of SHL, the 80-bits shift register is divided into two sections with each section having 40-bits. Data are then shifted into the shift register via D2_DL and D3_DM, or D3_DM and D4_DR. Please refer to Table 6 and Table 7.
80-bit level shifter	SEG	This block translates signals from logical voltage to high voltage for driving the STN LCD panel.
80-bit 4-level driver	SEG	Selects output voltage levels according to M and the latched data value.

4 PINNING DIAGRAMS

4.1 Pinning diagram of LQFP100 package

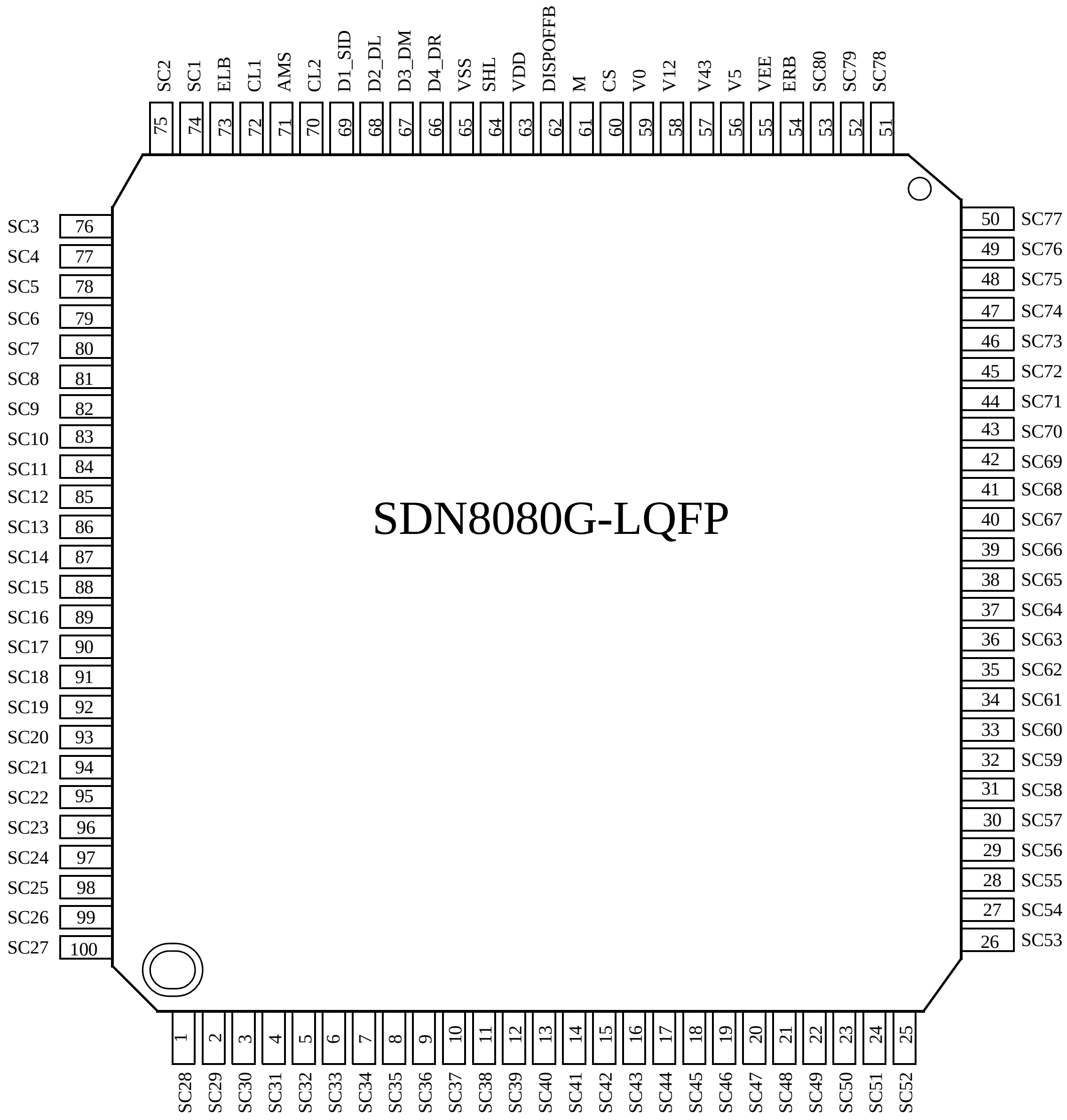


Fig.2 Pin assignment of the LQFP100 package.

4.2 Pinning diagram of QFP100 package

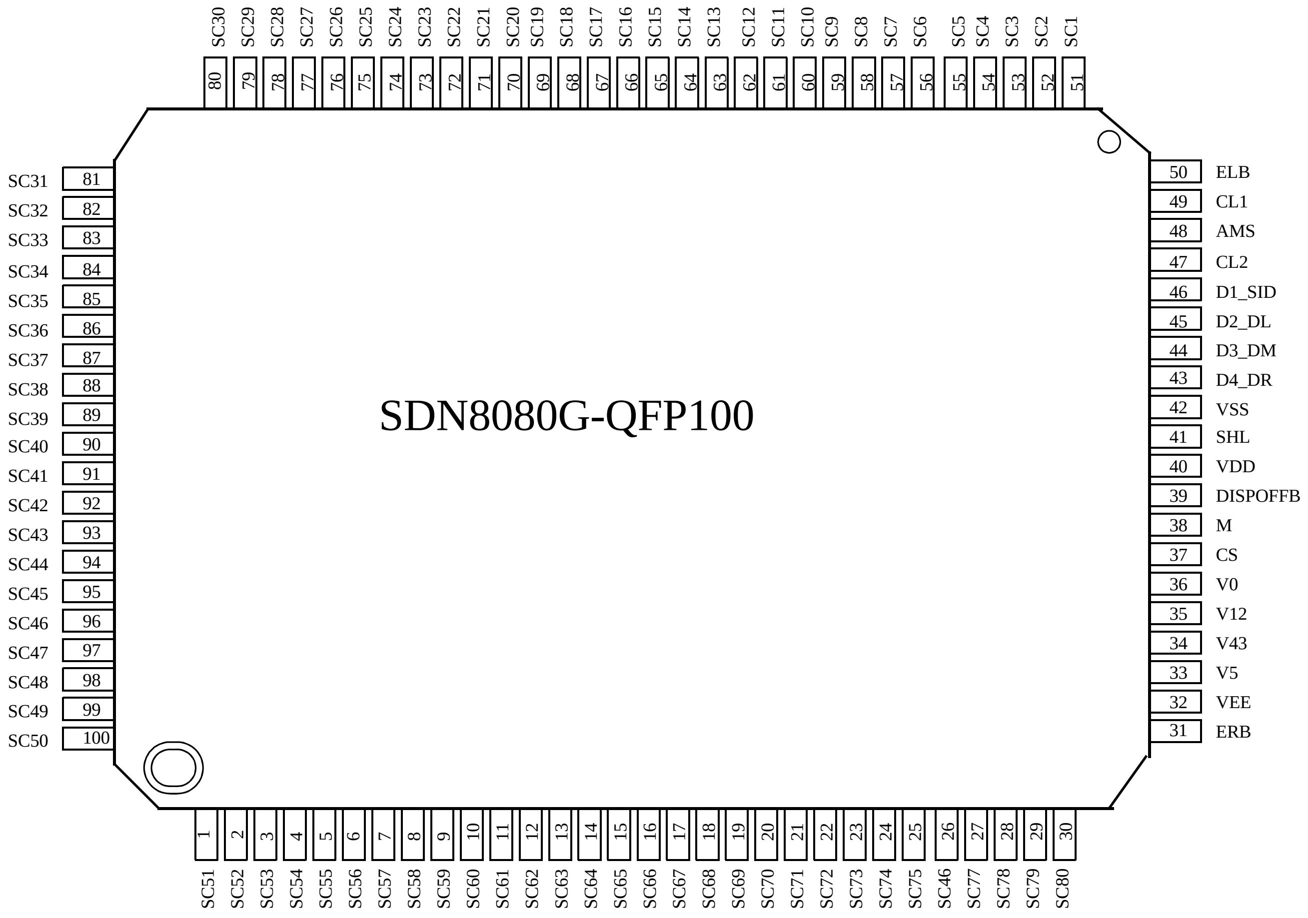
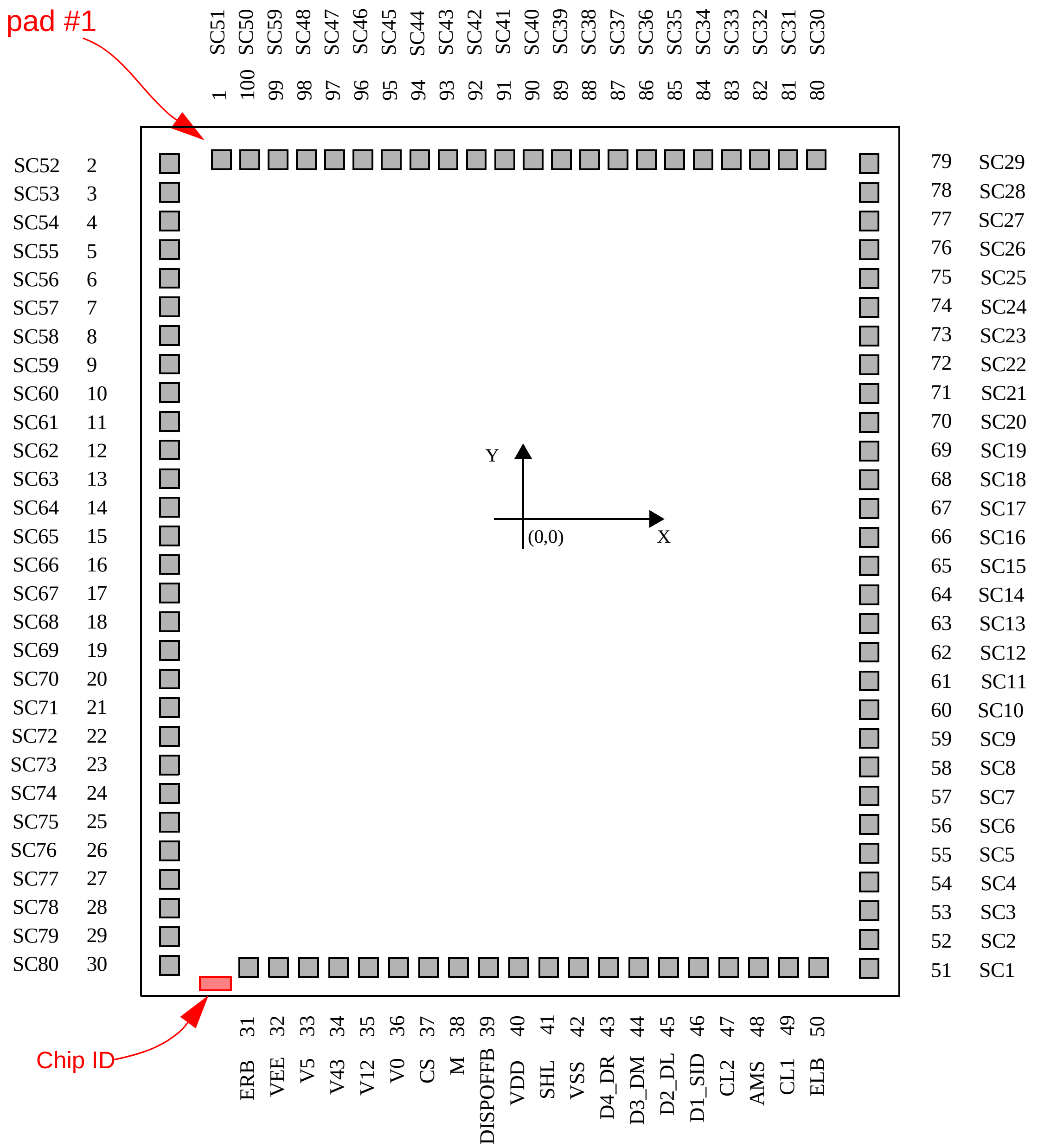


Fig.3 Pin assignment of the QFP100 package

4.3 Pad diagram



Note:

1. For chip_on_board (COB) bonding, chip carrier should be connected to VDD or left open. Chip carrier is the metal pad to which die is attached.
2. The chip size is : 2775 µm x 3169 µm.
3. The Chip ID is: 30001.

Fig.4 Pad locations.

4.4 Pad description

Table 3 Pad signal names and coordinates

The unit for coordinates is µm.

PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES		PAD NO.	PAD NAME	COORDINATES	
		X	Y			X	Y			X	Y
1	SC51	-1103	1467	35	V12	-565	-1472	69	SC19	1280	409
2	SC52	-1280	1459	36	V0	-456	-1472	70	SC20	1280	514
3	SC53	-1280	1354	37	CS	-331	-1472	71	SC21	1280	619
4	SC54	-1280	1249	38	M	-224	-1472	72	SC22	1280	724
5	SC55	-1280	1144	39	DISPOFFB	-118	-1472	73	SC23	1280	829
6	SC56	-1280	1039	40	VDD	-12	-1472	74	SC24	1280	934
7	SC57	-1280	934	41	SHL	95	-1472	75	SC25	1280	1039
8	SC58	-1280	829	42	VSS	208	-1472	76	SC26	1280	1144
9	SC59	-1280	724	43	D4_DR	321	-1472	77	SC27	1280	1249
10	SC60	-1280	619	44	D3_DM	427	-1472	78	SC28	1280	1354
11	SC61	-1280	514	45	D2_DL	534	-1472	79	SC29	1280	1459
12	SC62	-1280	409	46	D1_SID	640	-1472	80	SC30	1102	1467
13	SC63	-1280	304	47	CL2	746	-1472	81	SC31	997	1467
14	SC64	-1280	199	48	AMS	853	-1472	82	SC32	892	1467
15	SC65	-1280	94	49	CL1	959	-1472	83	SC33	787	1467
16	SC66	-1280	-11	50	ELB	1065	-1472	84	SC34	682	1467
17	SC67	-1280	-116	51	SC1	1280	-1482	85	SC35	577	1467
18	SC68	-1280	-221	52	SC2	1280	-1376	86	SC36	472	1467
19	SC69	-1280	-326	53	SC3	1280	-1271	87	SC37	367	1467
20	SC70	-1280	-431	54	SC4	1280	-1166	88	SC38	262	1467
21	SC71	-1280	-536	55	SC5	1280	-1061	89	SC39	157	1467
22	SC72	-1280	-641	56	SC6	1280	-956	90	SC40	52	1467
23	SC73	-1280	-746	57	SC7	1280	-851	91	SC41	-53	1467
24	SC74	-1280	-851	58	SC8	1280	-746	92	SC42	-158	1467
25	SC75	-1280	-956	59	SC9	1280	-641	93	SC43	-263	1467
26	SC76	-1280	-1061	60	SC10	1280	-536	94	SC44	-368	1467
27	SC77	-1280	-1166	61	SC11	1280	-431	95	SC45	-473	1467
28	SC78	-1280	-1271	62	SC12	1280	-326	96	SC46	-578	1467
29	SC79	-1280	-1376	63	SC13	1280	-221	97	SC47	-683	1467
30	SC80	-1280	-1481	64	SC14	1280	-116	98	SC48	-788	1467
31	ERB	-1016	-1472	65	SC15	1280	-11	99	SC49	-893	1467
32	VEE	-894	-1472	66	SC16	1280	94	100	SC50	-998	1467
33	V5	-784	-1472	67	SC17	1280	199				
34	V43	-678	-1472	68	SC18	1280	304				

4.5 Signal description

Table 4 Pad signal description.

To avoid a latch-up effect at power-on: V_{SS} – 0.5 V < voltage at any pin at any time < V_{DD} + 0.5 V .

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>Interface to/from</th><th>DESCRIPTION</th></tr>
<tr><td>V0, V12, V43, V5</td><td>input</td><td>power</td><td>External bias voltage for LCD driver.</td></tr>
<tr><td>SC1~SC80</td><td>output</td><td>LCD</td><td>SEGMENT or COMMON driver outputs.</td></tr>
<tr><td>CL2</td><td>input</td><td>controller</td><td>In SEGMENT driver application mode, CL2 is the shifting clock of the 20 x 4-bit bi-directional shift register.
In COMMON driver application mode, this clock is not used. The display data is shifted to the 80-bit COMMON data bi-directional shift register by CL1.
This input has an internal pull-high PMOS. When the device is used as COMMON driver, the PMOS is turned on to internally pull this input to HIGH and this pin should therefore be left open or connected to VDD. Please refer to Section 13.</td></tr>
<tr><td>M</td><td>input</td><td>controller</td><td>Alternating signal for generating alternating LCD-bias voltage.</td></tr>
<tr><td>CL1</td><td>input</td><td>controller</td><td>In SEGMENT driver application mode, the 80-bits display data is latched into the shift register at the falling edge of this clock.
In COMMON driver application mode, CL1 is used as shifting clock of COMMON output data.</td></tr>
<tr><td>DISPOFFB</td><td>input</td><td>controller</td><td>During the LOW period of this signal, V0 is selected as SC0~SC80’s outputs and the display is therefore turned off.</td></tr>
<tr><td>CS</td><td>input</td><td>VDD/VSS</td><td>If CS is connected to VSS, the SDN8080G is used as an 80-output SEGMENT driver.
If CS is connected to VDD, the SDN8080G is used as an 80-output COMMON driver.</td></tr>
<tr><td>AMS</td><td>input</td><td>VDD/VSS</td><td>Application Mode Selection.
Together with CS input, this input is used to configure SDN8080G into different application modes, as shown in the following table.
<table>
<tr><th>CS</th><th>AMS</th><th>application mode</th><th>COM/SEG</th></tr>
<tr><td>0</td><td>0</td><td>4-bit parallel data interface with a controller.</td><td rowspan="2">SEG</td></tr>
<tr><td>0</td><td>1</td><td>1-bit serial data interface with a controller.</td></tr>
<tr><td>1</td><td>0</td><td>Single-type application mode</td><td rowspan="2">COM</td></tr>
<tr><td>1</td><td>1</td><td>Dual-type application mode</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>SYMBOL</th><th>I/O</th><th>Interface to/from</th><th>DESCRIPTION</th></tr>
<tr><td>D1_SID,
D2_DL,
D3_DM,
D4_DR</td><td>I/O,
D2,
D4.
Input,
D1,
D3</td><td>controller</td><td>In SEGMENT Driver mode and when 4-bit parallel data interface mode is selected, these 4 inputs are used as 4-bit parallel data input from a controller.
In SEGMENT driver mode and when 1-bit serial interface mode is selected, D1_SID is used as serial data input from a controller. In this application, all other 3 inputs must be connected to VDD.
In COMMON driver mode and when single-type application mode is selected, COMMON scan pulse is shifted from D2_DL to D4_DR or from D4_DR to D2_DL, depending on the logic state of SHL.
In COMMON driver mode and when dual-type application mode is selected, COMMON scan pulse is shifted from D2_DL and D3_DM to D4_DR, or from D4_DR and D3_DM to D2_DL, depending on the logic state of SHL.</td></tr>
<tr><td>SHL</td><td>input</td><td>VDD/VSS</td><td>Shift direction control.
When this input is connected to VSS, data shift direction is from left to right. When this input is connected to VDD, data shift direction is from right to left. Please refer to Table 6 and Table 7.</td></tr>
<tr><td>ELB, ERB</td><td>input/
output</td><td>cascade</td><td>In order to reduce power consumption, in SEGMENTdriver application mode, the internal operation of the SDN8080G is enabled only when its enable input (ELB or ERB) is at “LOW”. When several SDN8080G are connected in cascade, their enable inputs(ELB or ERB) are serially enabled. The enabling sequence is decided by SHL, as listed below.
<table>
<tr><th rowspan="2">SHL</th><th colspan="2">Segment Driver</th></tr>
<tr><th>ELB</th><th>ERB</th></tr>
<tr><td>L</td><td>Output</td><td>Input</td></tr>
<tr><td>H</td><td>Input</td><td>Output</td></tr>
</table>
In COMMON driver application, these two pins are not used and should be left open.</td></tr>
</table>

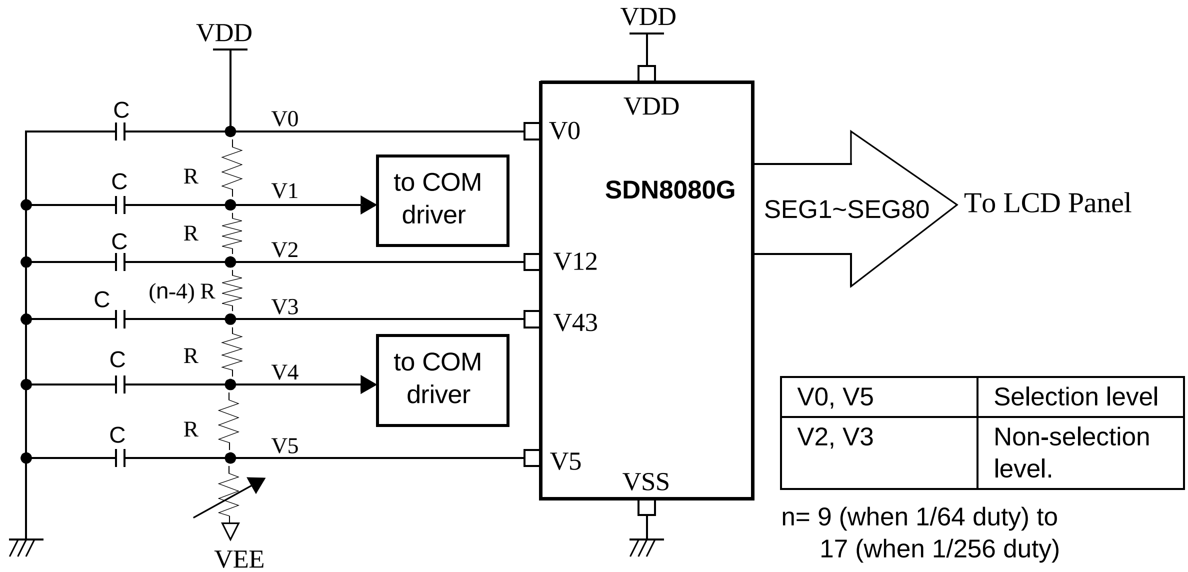
5 OUTPUT VOLTAGE LEVEL

Table 5 Output voltage level

M	LATCHED DATA	DISPOFFB	OUTPUT LEVEL(SC1-SC80) SEGMENT MODE	OUTPUT LEVEL(SC1-SC80) COMMON MODE
L	L	H	V12(V2)	V12(V1)
L	H	H	V0	V5
H	L	H	V43(V3)	V43(V4)
H	H	H	V5	V0
x(don't care)	x(don't care)	L	V0	V0

6 LCD BIAS VOLTAGE

6.1 SEGMENT driver application (CS=LOW)



V0, V5	Selection level
V2, V3	Non-selection level.

n= 9 (when 1/64 duty) to
17 (when 1/256 duty)

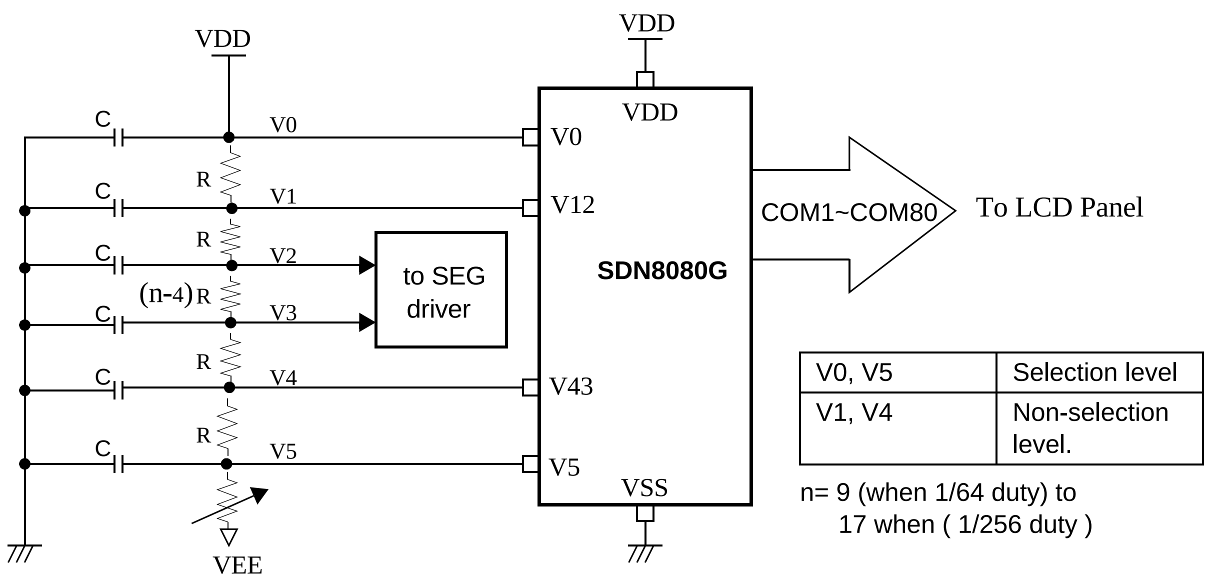
Note:

(1) The recommended value for R is in the range from 1K to 10K ohm.

(2) The recommended value for C is 0.1 μF.

Fig.5 SEGMENT driver application.

6.2 COMMON driver application (CS=HIGH)



V0, V5	Selection level
V1, V4	Non-selection level.

n= 9 (when 1/64 duty) to
17 when (1/256 duty)

Note:

(1) The recommended value for R is in the range from 1K to 10K ohm.

(2) The recommended value for C is 0.1 μF.

Fig.6 COMMON driver application.

7 DATA SHIFT DIRECTION AND DATA PIN I/O SELECTION

Table 6 Data shift direction in SEGMENT driver application (CS=LOW).

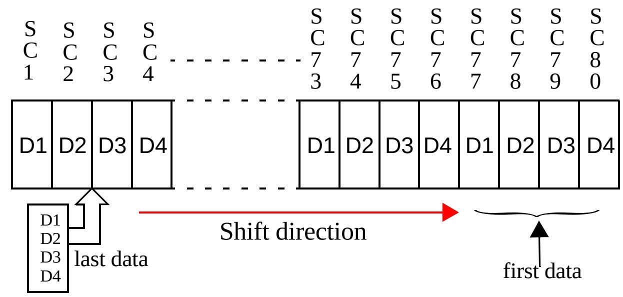
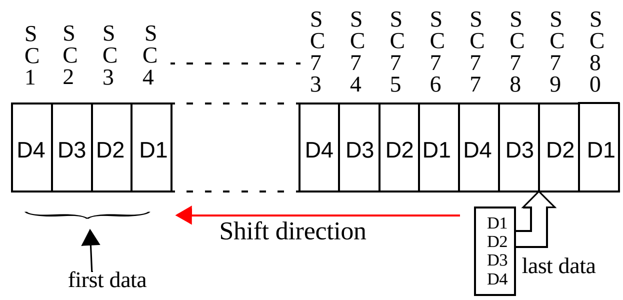
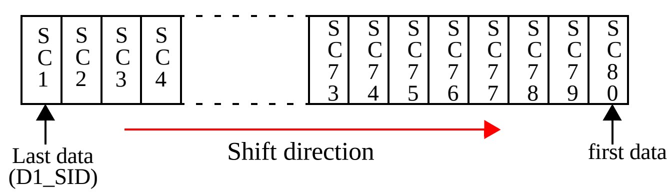
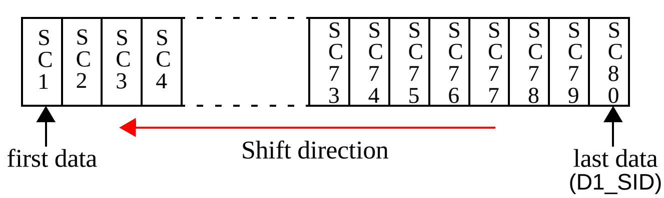
<table>
<tr><th>AMS</th><th>SHL</th><th>Application mode</th><th>DATA SHIFT DIRECTION</th><th>INPUT PIN(PAD)</th></tr>
<tr><td rowspan="2">L</td><td>L</td><td rowspan="2">4-bit parallel data interface mode</td><td>
</td><td rowspan="2">D1_SID,
D2_DL,
D3_DM,
D4_DR</td></tr>
<tr><td>H</td><td>
</td></tr>
<tr><td rowspan="2">H</td><td>L</td><td rowspan="2">1-bit serial data interface mode</td><td>
</td><td rowspan="2">D1_SID</td></tr>
<tr><td>H</td><td>
</td></tr>
</table>

Table 7 Data shift direction in COMMON driver application (CS=HIGH)

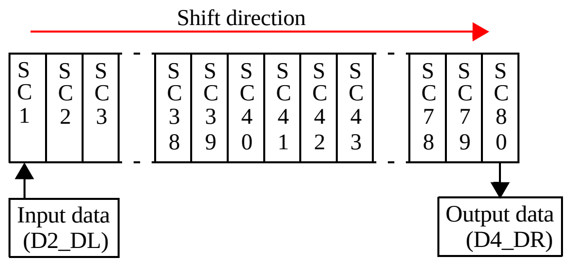
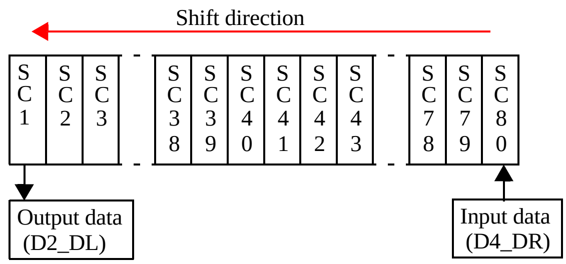
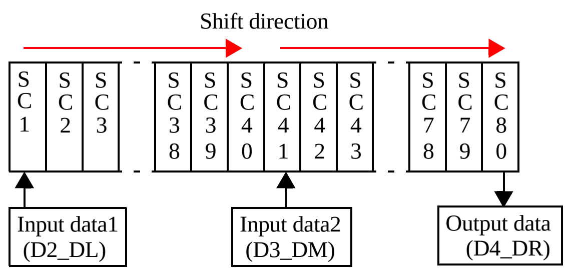
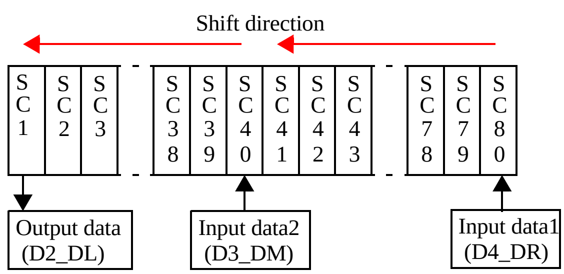
AMS	SHL	Application mode	DATA SHIFT DIRECTION	Input pin(pad)
L	L	Single-type application mode		D2_DL
	H			D4_DR
H	L	dual-type application mode		D2_DL, D3_DM
	H			D4_DR, D3_DM

Table 8 Application of I/O data pins D1_SID, D2_DL, D3_DM, and D4_DR.

<table>
<tr><td rowspan="2">COM/SEG
(CS pin)</td><td rowspan="2">Application mode
(AMS pin)</td><td rowspan="2">SHL</td><td colspan="4">Data interface pins</td></tr>
<tr><td>D1_SID</td><td>D2_DL</td><td>D3_DM</td><td>D4_DR</td></tr>
<tr><td rowspan="2">SEG
(CS=LOW)</td><td>4-bit parallel interface mode (AMS=LOW)</td><td>X</td><td>D1 (input)</td><td>D2 (input)</td><td>D3 (input)</td><td>D4 (input)</td></tr>
<tr><td>1-bit serial interface mode (AMS=HIGH)</td><td>X</td><td>D1_SID</td><td colspan="3">connected to VDD.</td></tr>
<tr><td rowspan="4">COM
(CS=HIGH)</td><td rowspan="2">single-type application mode (AMS=LOW)</td><td>L</td><td rowspan="2">Open</td><td>D2_DL (input)</td><td rowspan="2">open</td><td>D4_DR (output)</td></tr>
<tr><td>H</td><td>D2_DL (output)</td><td>D4_DR (input)</td></tr>
<tr><td rowspan="2">dual-type application mode (AMS=HIGH)</td><td>L</td><td rowspan="2">Open</td><td>D2_DL (input1)</td><td>D3_DM (input2)</td><td>D2_DR (output2)</td></tr>
<tr><td>H</td><td>D2_DL (output2)</td><td>D3_DM (input2)</td><td>D4_DR (input1)</td></tr>
</table>

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute maximum rating

Table 9 Absolute maximum rating

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	voltage on the VDD input.	–0.3	+7.0	V
V_{LCD}	voltage difference between VDD and VEE.	0.0	+30.0	V
V_I (note 1)	input voltage on any pin with respect to V_{SS}	–0.3	V_{DD} + 0.3	V
I_I, I_O	input/output current on any I/O pin	–	±15	mA
P_{tot}	total power dissipation (note 2)	–	1.5	W
T_{stg}	storage temperature range	–55	+150	°C
T_{amb}	operating ambient temperature range.	-30	+ 85	°C

Notes

1. The following applies to the Absolute Maximum Ratings:
   a) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.
   b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effect of excessive static charge. However, it is suggested that conventional precautions be taken to avoid applying greater than the rated maxima.
   c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package, not on device power consumption.

8.2 DC characteristics for SEGMENT driver application

Table 10 DC Characteristics for SEGMENT driver application

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = –30 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	Control logic circuit	2.7	5.5	V
V_{LCD}	supply voltage for LCD	V_{LCD}= VDD - VEE	6	28	V
V_{IL}	LOW level input voltage	note 1	0	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.8V_{DD}$	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 0.4 mA; note 2	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = -0.4 mA; note 2	$V_{DD} - 0.4$		V
I_{LI1}	input leakage current of input pins	note 1	–10	10	μA
I_{LI2}	input leakage current of V0~V5	note 3	–25	+25	μA
I_{STBY}	Standby current at VDD=5 volts	note 4		100	μA
I_{STBY}	Standby current at VDD=3 volts	note 5		100	μA
$I_{DD(VDD=5V)}$	Operating current at VDD=5 volts	note 6		5	mA
$I_{DD(VDD=3V)}$	Operating current at VDD=3 volts	note 7		2	mA
I_{EE}	High-voltage operating current.	note 8		500	μA
R_{ON}	ON resistance	I_{ON}= 100μA, note 9	2K (typ.), 4K (max.)		Ω

Notes to the DC characteristics:

1. Measured for the following pins: CL1, CL2, ELB, ERB, D1_SID, D2_DL, D3_DM, D4_DR, SHL, DISPOFFB, M, CS, and AMS.
2. Measured for the ERB pin and the ELB pin.
3. Measured for V0, V12, V43, and V5.
4. Conditions for the measurement: VDD=5V, V0=VDD, V12=1.71 V, V43= -19.71 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=5.12 MHz, SHL=VSS, DISPLAYOFFB=VDD, M=VSS, AMS=0, no-load condition (1/256 duty, 1/17 bias), display data pattern= 0000.
5. Conditions for the measurement: VDD=3V, V0=VDD, V12=-0.06 V, V43= -19.94 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=5.12 MHz, SHL=VSS, DISPLAYOFFB=VDD, M=VSS, AMS=0, no-load condition (1/256 duty, 1/17 bias), display data pattern= 0000.
6. Conditions for the measurement: VDD=5V, V0=VDD, V12=1.71 V, V43= -19.71 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=5.12 MHz, SHL=VSS, DISPLAYOFFB=VDD, F_M=80 Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), display data pattern= 01010.
7. Conditions for the measurement: VDD=3V, V0=VDD, V12=-0.06 V, V43= -19.94 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=4 MHz, SHL=VSS, DISPLAYOFFB=VDD, F_M=80 Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), display data pattern= 01010.
8. Conditions for the measurement: VDD=5V, V0=VDD, V12=1.71 V, V43= -19.71 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=5.12 MHz, SHL=VSS, DISPLAYOFFB=VDD, F_M=80 Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), display data pattern= 01010. Measured at VEE pin.
9. Conditions for the measurement: VLCD=VDD-VEE, V0=VDD=5V, V5=VEE=-23V, V12= VDD - (2/N) x VLCD, V43=VEE + (2/N) x VLCD, N=17 (1/256 duty, 1/17 bias).

8.3 DC characteristics for COMMON driver application

Table 11 DC Characteristics for COMMON driver application

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = –30 to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	Control logic part	2.7	5.5	V
V_{LCD}	supply voltage for LCD	V_{LCD}= VDD - VEE	6	28	V
V_{IL}	LOW level input voltage	note 1	0	$0.2V_{DD}$	V
V_{IH}	HIGH level input voltage	note 1	$0.8V_{DD}$	V_{DD}	V
V_{OL}	LOW level output voltage	I_{OL} = 0.4 mA; note 2	–	0.4	V
V_{OH}	HIGH level output voltage	I_{OH} = -0.4 mA; note 2	$V_{DD} - 0.4$		V
I_{LI1}	input leakage current of input pins	note 1	–10	10	μA
I_{LI2}	input leakage current of V0~V5 pins	note 3	–25	+25	μA
I_{LI3}	input leakage current of input pins with internal pull-up MOS.	note 4	–25	+25	μA
I_{STBY}	Standby current at VDD=5 volts	note 5		100	μA
I_{STBY}	Standby current at VDD=3 volts	note 6		100	μA
$I_{DD(VDD=5V)}$	Operating current at VDD=5 volts	note 7		200	μA
$I_{DD(VDD=3V)}$	Operating current at VDD=3 volts	note 8		120	μA
I_{EE}	High-voltage operating current.	note 9		500	μA
R_{ON}	ON resistance	I_{ON}= 100μA, note 10	2K (typ.), 4K (max.)		Ω

Notes to the DC characteristics

1. Measured for the following input pins: CL1, D2_DL(when SHL=LOW), D4_DR(when SHL=HIGH), SHL, DISPOFFB, M, CS, and AMS.
2. Measured for the following output pins: D2_DL(when SHL=HIGH) and D4_DR(when SHL=LOW).
3. Measured for V0, V12, V43, and V5.
4. Measured for the following input pins with internal pull-up: CL2, D1_SID, D3_DM(AMS=HIGH), ELB(SHL=LOW), ERB(SHL=HIGH).
5. Conditions for the measurement: VDD=5V, V0=VDD, V12=3.35 V, V43= -21.35 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=disabled, SHL=VSS, DISPLAYOFFB=VDD, D2_DL=M=VSS, AMS=0, no-load condition (1/256 duty, 1/17 bias), D1_SID=D3_DM=VDD, D4_DR=ELB=ERB=OPEN.
6. Conditions for the measurement: VDD=5V, V0=VDD, V12=1.47 V, V43= -21.47 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=disabled, SHL=VSS, DISPLAYOFFB=VDD, D2_DL=M=VSS, AMS=0, no-load condition (1/256 duty, 1/17 bias), D1_SID=D3_DM=VDD, D4_DR=ELB=ERB=OPEN.
7. Conditions for the measurement: VDD=5V, V0=VDD, V12=3.35 V, V43= -21.35 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=disabled, SHL=VSS, DISPLAYOFFB=VDD, D2_DL=VDD, f_M=80Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), D1_SID=D3_DM=VDD, D4_DR=ELB=ERB=OPEN.
   Display data pattern= 10000000..., 01000000..., 00100000..., 00010000.
8. Conditions for the measurement: VDD=3V, V0=VDD, V12=1.47 V, V43= -21.47 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=disabled, SHL=VSS, DISPLAYOFFB=VDD, D2_DL=VDD, f_M=80Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), D1_SID=D3_DM=VDD, D4_DR=ELB=ERB=OPEN.
   Display data pattern= 10000000..., 01000000..., 00100000..., 00010000.
9. Conditions for the measurement: VDD=5V, V0=VDD, V12=3.35 V, V43= -21.35 V, V5=VEE= -23 V, F_{CL1}=32 KHz, F_{CL2}=disabled, SHL=VSS, DISPLAYOFFB=VDD, D2_DL=VDD, f_M=80Hz, AMS=0, no-load condition (1/256 duty, 1/17 bias), D1_SID=D3_DM=VDD, D4_DR=ELB=ERB=OPEN.

Display data pattern= 10000000..., 01000000..., 00100000..., 00010000.
Measured at the VEE pin (that is, current flowing through the VEE pad).

10. VLCD= VDD-VEE, V0=VDD=5 volts, V5=VEE=-23 volts. V12= VDD- (1/N) x VLCD, V43= VEE+ (1/N) x VLCD, N=17(1/256 duty, 1/17 bias).

8.4 AC characteristics for SEGMENT driver application

Table 12 AC characteristics for SEGMENT driver application

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -30 °C to +85°C.

SYMBOL	PARAMETER	VDD=5V±10%			VDD=3V±10%			Test condition	UNIT
		MIN.	TYP	MAX.	MIN.		MAX.		
t_{CY}	Clock cycle time	125			250			Duty=50%	ns
t_{WCK}	Clock pulse width	45			95				ns
t_R, t_F	Clock rise/fall time			30			30		ns
t_{DS}	Data set-up time	30			65				ns
t_{DH}	Data hold time	30			65				ns
t_{CS}	Clock set-up time	80			120				ns
t_{CH}	Clock hold time	80			120				ns
t_{PHL}	Propagation delay time (ELB output)			60			125		ns
t_{PHL}	Propagation delay time (ERB output)			60			125		ns
t_{PSU}	ELB set-up time	30			65			ELB input	ns
t_{PSU}	ERB set-up time	30			65			ERB input	ns
t_{WDL}	DISPOFFB low pulse width	1200			1200				ns
t_{CD}	DISPOFFB clear time	100			100				ns
t_{PD1}	M - OUT propagation delay time			1000			1200	C_L= 15 pF	ns
t_{PD2}	CL1 - OUT propagation delay time			1000			1200	C_L= 15 pF	ns
t_{PD3}	DISPOFFB - OUT propagation delay time			1000			1200	C_L= 15 pF	ns

8.5 AC characteristics for COMMON driver application

Table 13 AC characteristics for COMMON driver application

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = -30 °C to +85°C.

SYMBOL	PARAMETER	VDD=5V±10%			VDD=3V±10%			Test condition	UNIT
		MIN.	TYP	MAX.	MIN.		MAX.		
t_{CY}	Clock cycle time	250			500			Duty=50%	ns
t_{WCK}	Clock pulse width	45			95				ns
t_R, t_F	Clock rise/fall time			50			50		ns
t_{DS}	Data set-up time	30			65				ns
t_{DH}	Data hold time	30			65				ns
t_{WDL}	DISPOFFB low pulse width	1200			1200				ns
t_{CD}	DISPOFFB clear time	100			100				ns
t_{DL}	Output delay time			200			250	C_L= 15 pF	ns

SYMBOL	PARAMETER	VDD=5V±10%			VDD=3V±10%			Test condition	UNIT
		MIN.	TYP	MAX.	MIN.		MAX.		
t_{PD1}	M - OUT propagation delay time			1000			1200	C_L= 15 pF	ns
t_{PD2}	CL1 - OUT propagation delay time			1000			1200	C_L= 15 pF	ns
t_{PD3}	DISPOFFB - OUT propagation delay time			1000			1200	C_L= 15 pF	ns

9 TIMING DIAGRAM

9.1 Timing diagram for SEGMENT driver application

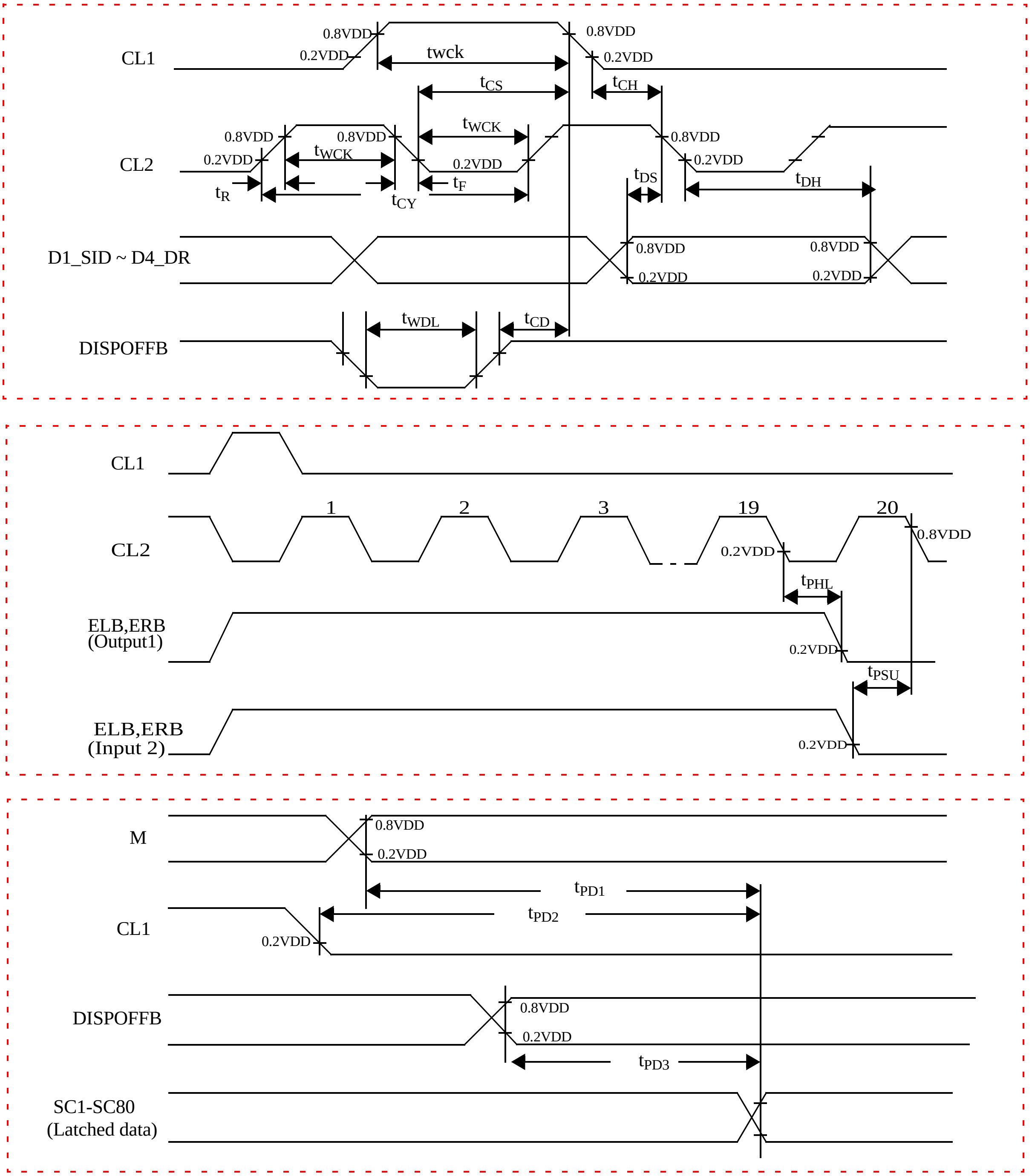
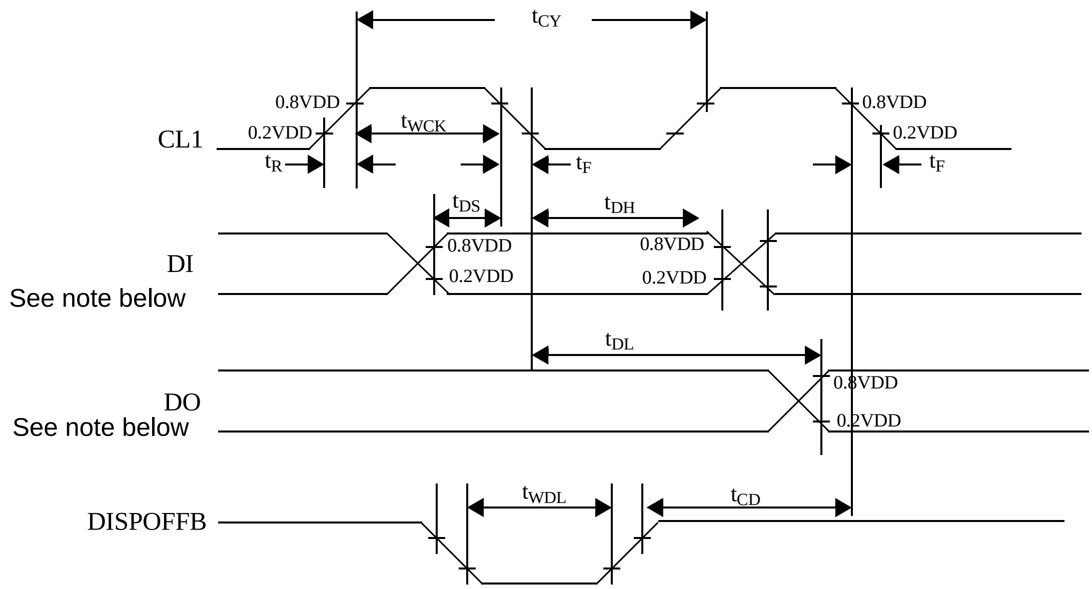


Fig.18 Timing diagram for SEGMENT driver application.

9.2 Timing diagram for COMMON driver application



Note:
When in single-type interface mode:
(1) DI=> D2_DL (SHL=L), D4_DR (SHL=H).
(2) DO=> D4_DR (SHL=L), D2_DL (SHL=H).
When in dual-type interface mode:
(3) DI=>D2_DL and D3_DM (SHL=L), D4_DR and D3_DM (SHL=H)
(4) DO=>D4_DR (SHL=L), D2_DL (SHL=H).

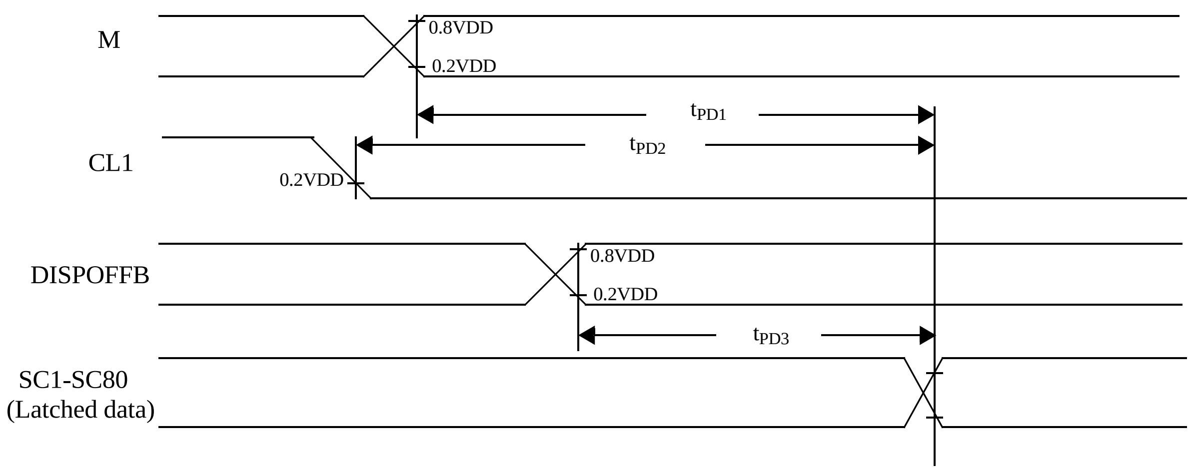


Fig.19 Timing diagram for COMMON driver application.

10 POWER DOWN FUNCTION

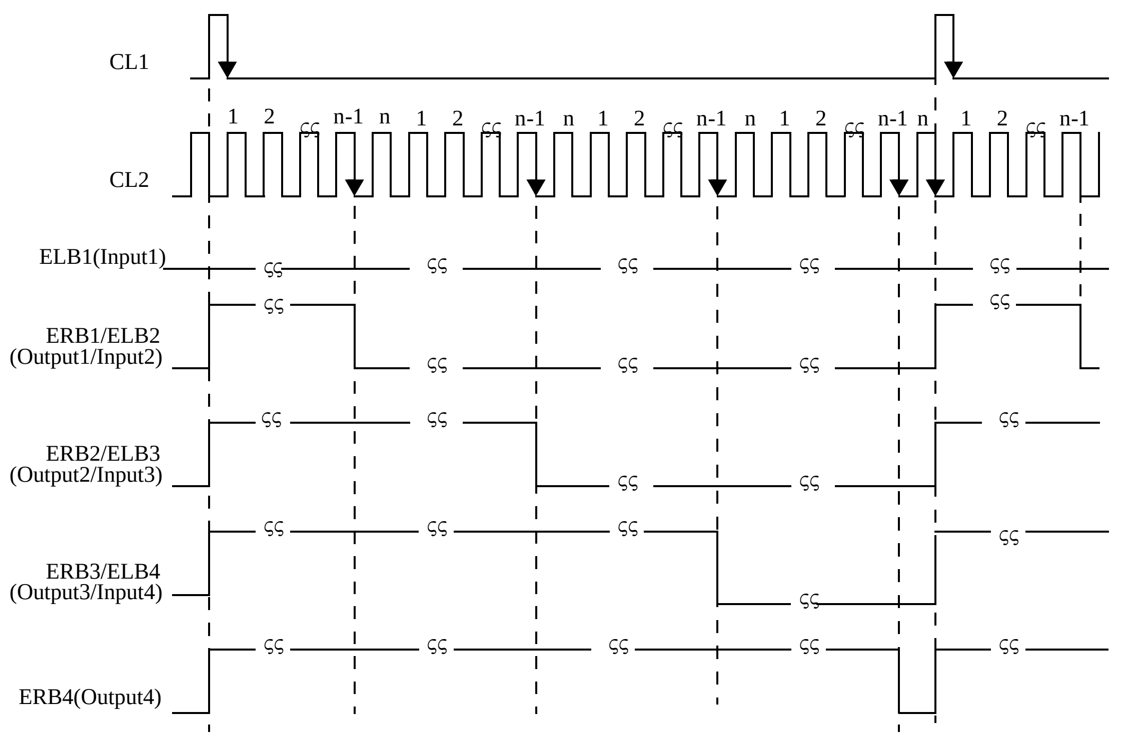
To reduce power consumption, the SDN8080G is sequentially enabled via POWER DOWN mode, when used in cascade in SEGMENT driver application.

Table 14 Power Down function.

SHL	Enable input	Enable output	current driver status (the driver being enabled)	status of other drivers
L	ERB	ELB	While ERB=LOW, current driver is enabled.	Disabled.
H	ELB	ERB	While ELB=LOW, current driver is enabled.	Disabled.

Note

1. Power Down function is not available when the SDN8080G is used as a COMMON driver.



Notes:

(1) SHL=HIGH (ELB=input, ERB=output). Current SDN8080G's ERB output must be connected to the next SDN8080G's ELB input.

(2) When in 4-bit parallel interface mode: n=20.

(3) When in 1-bit serial interface mode: n=80.

Fig.20 Timing diagram for Power Down function.

11 OPERATION TIMING DIAGRAM

11.1 4-bit parallel mode interface (SEGMENT driver)

11.1.1 WHEN SHL=LOW

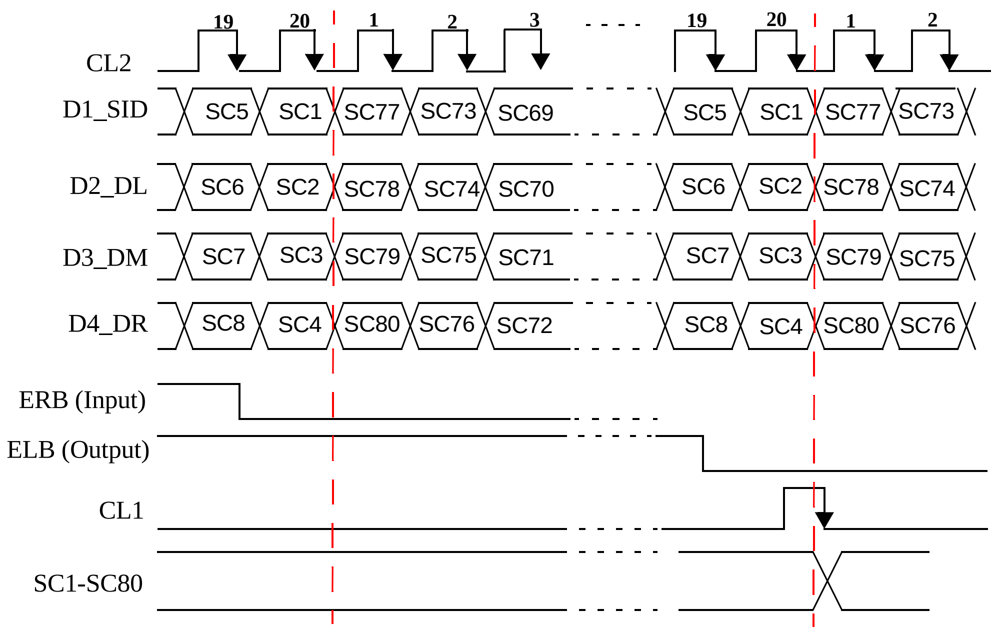


Fig.21 When SHL=LOW.

11.1.2 WHEN SHL=HIGH

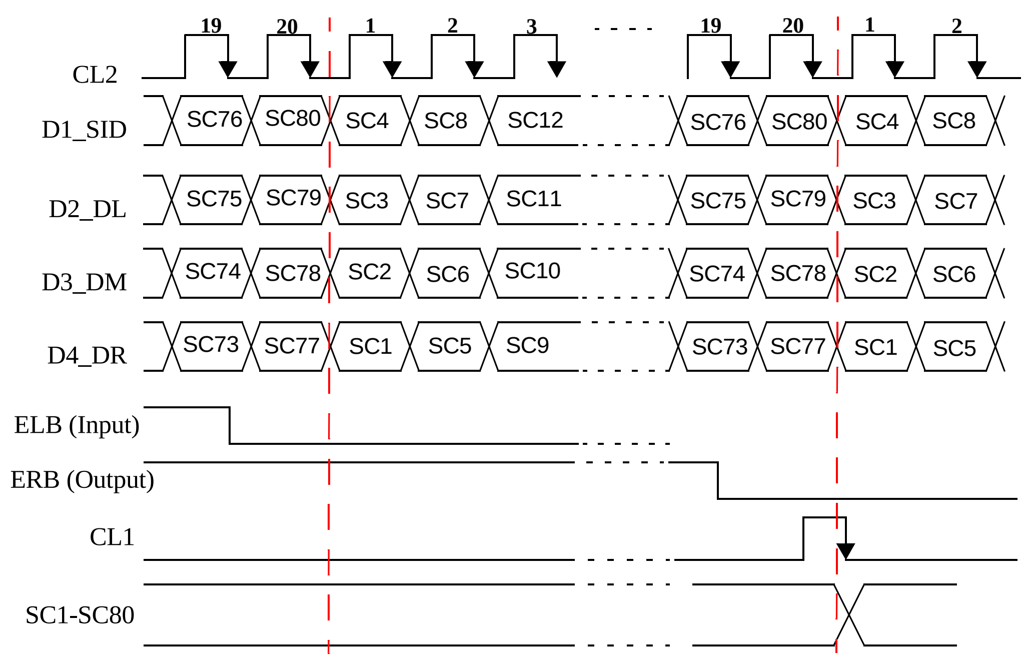


Fig.22 When SHL=HIGH

11.2 1-bit serial mode interface (SEGMENT driver)

11.2.1 WHEN SHL=LOW

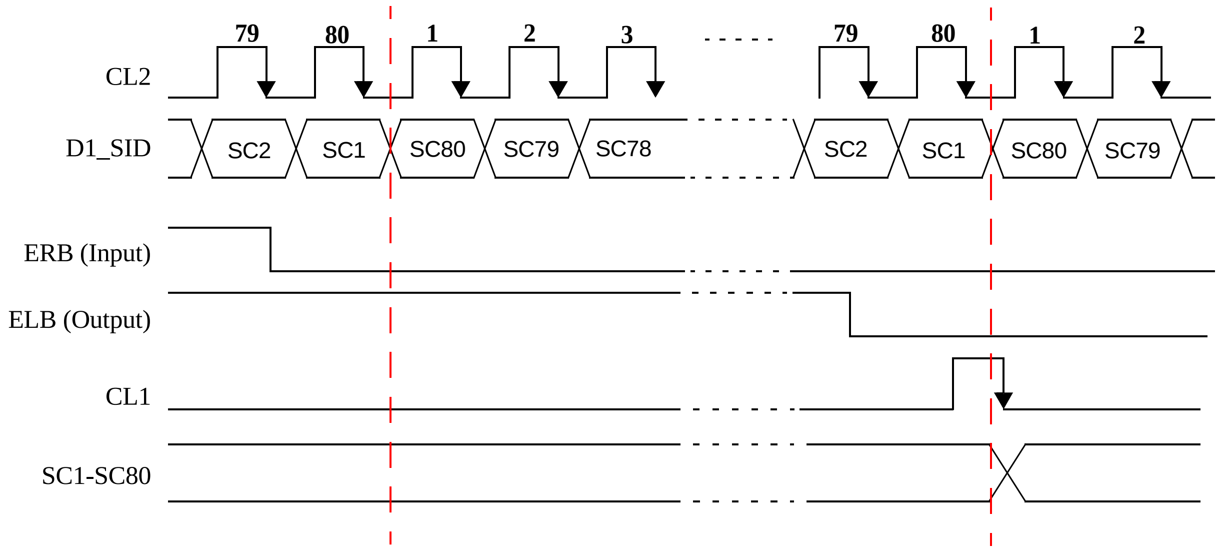


Fig.23 SHL=LOW, 1-bit serial mode interface.

11.2.2 WHEN SHL=HIGH

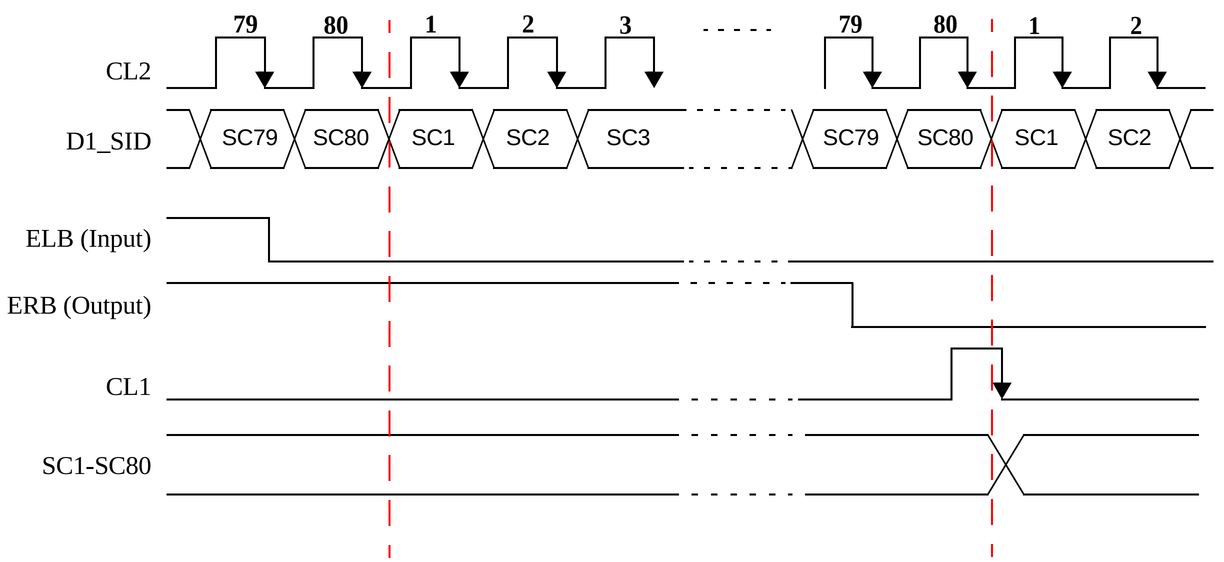


Fig.24 SHL=HIGH, 1-bit serial mode interface.

11.3 Single type interface mode (COMMON driver)

11.3.1 When SHL=LOW

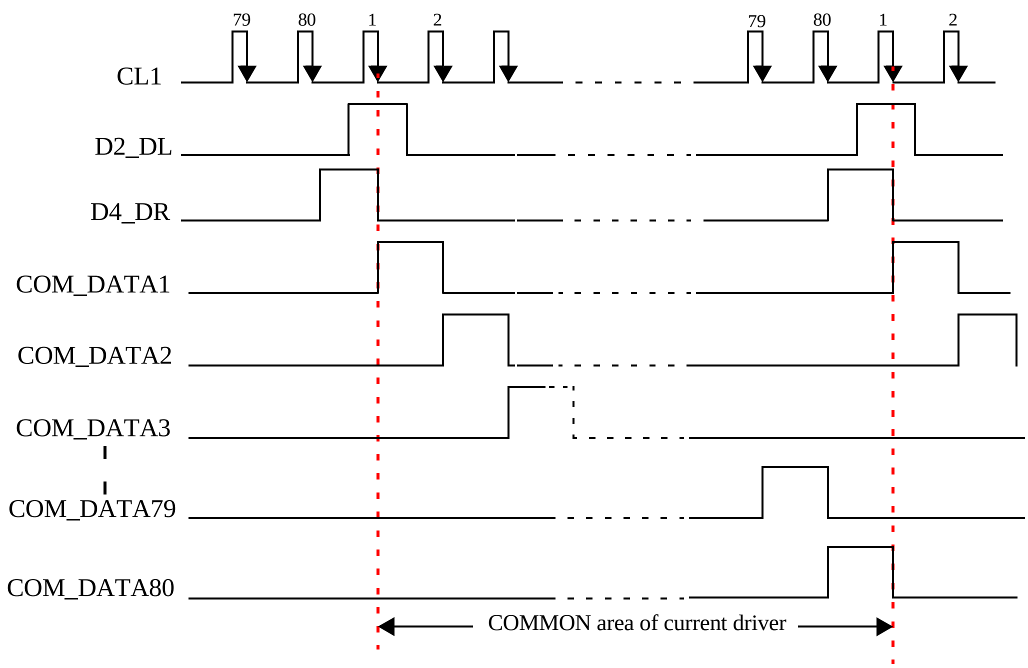


Fig.25 SHL=LOW, single-type interface mode.

11.3.2 When SHL=HIGH

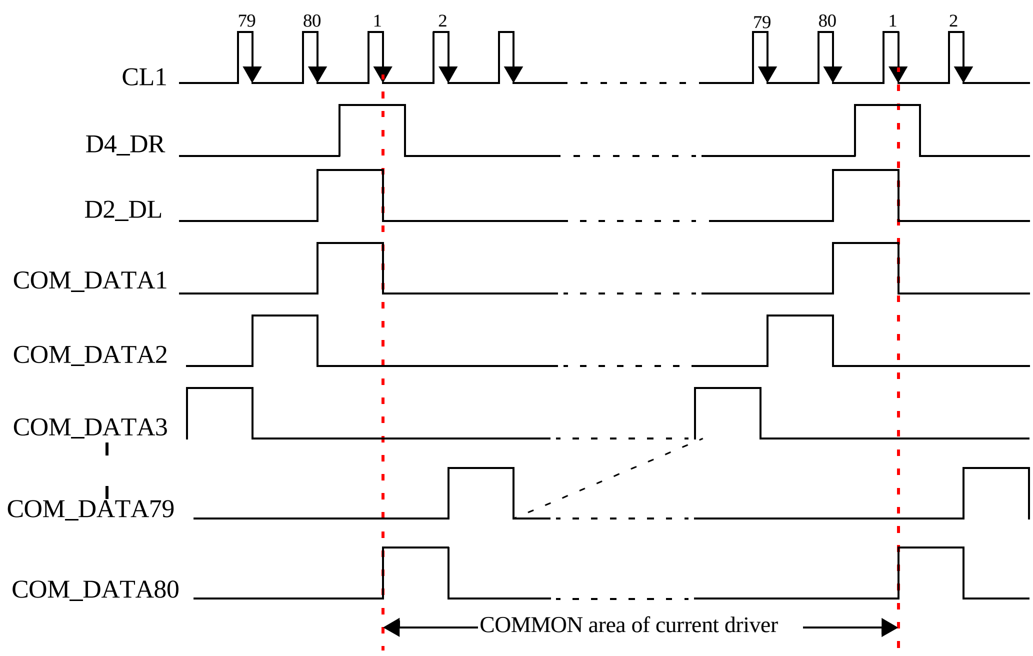


Fig.26 SHL=HIGH, single-type interface mode.

11.4 Dual type interface mode (COMMON driver)

11.4.1 When SHL=LOW

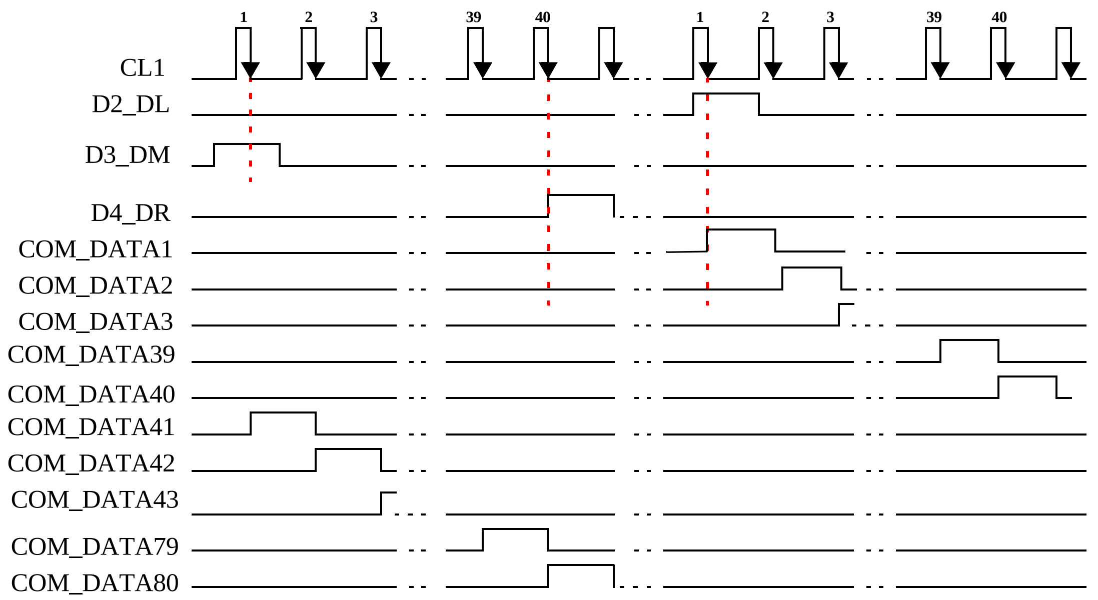


Fig.27 SHL=LOW, dual-type interface mode.

11.4.2 When SHL=HIGH

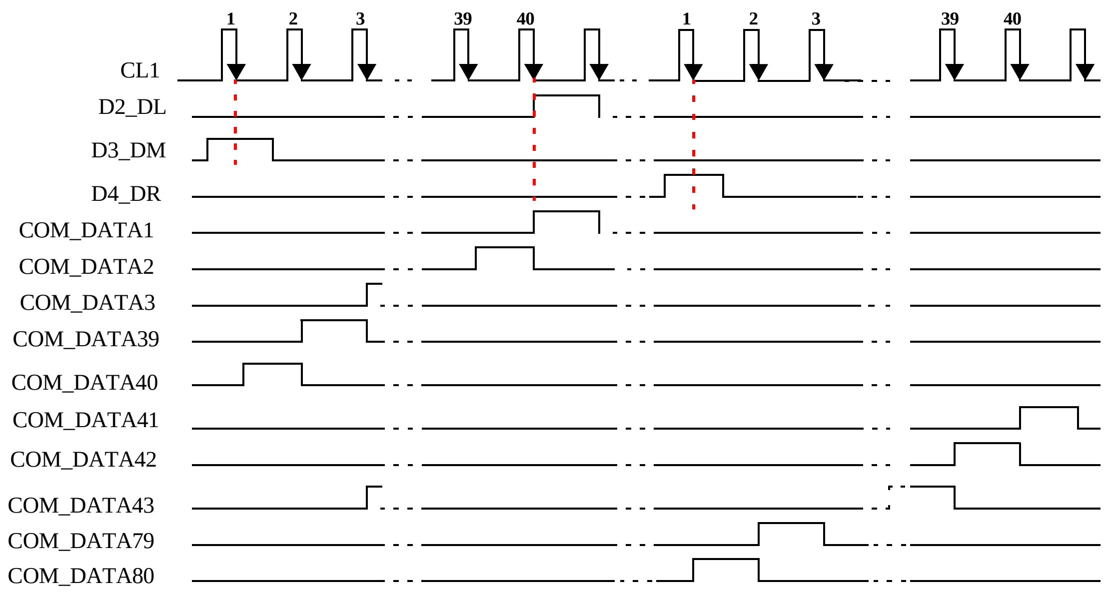


Fig.28 SHL=HIGH, dual-type interface mode.

11.5 COMMON/SEGMENT driver timing (1/200 duty)

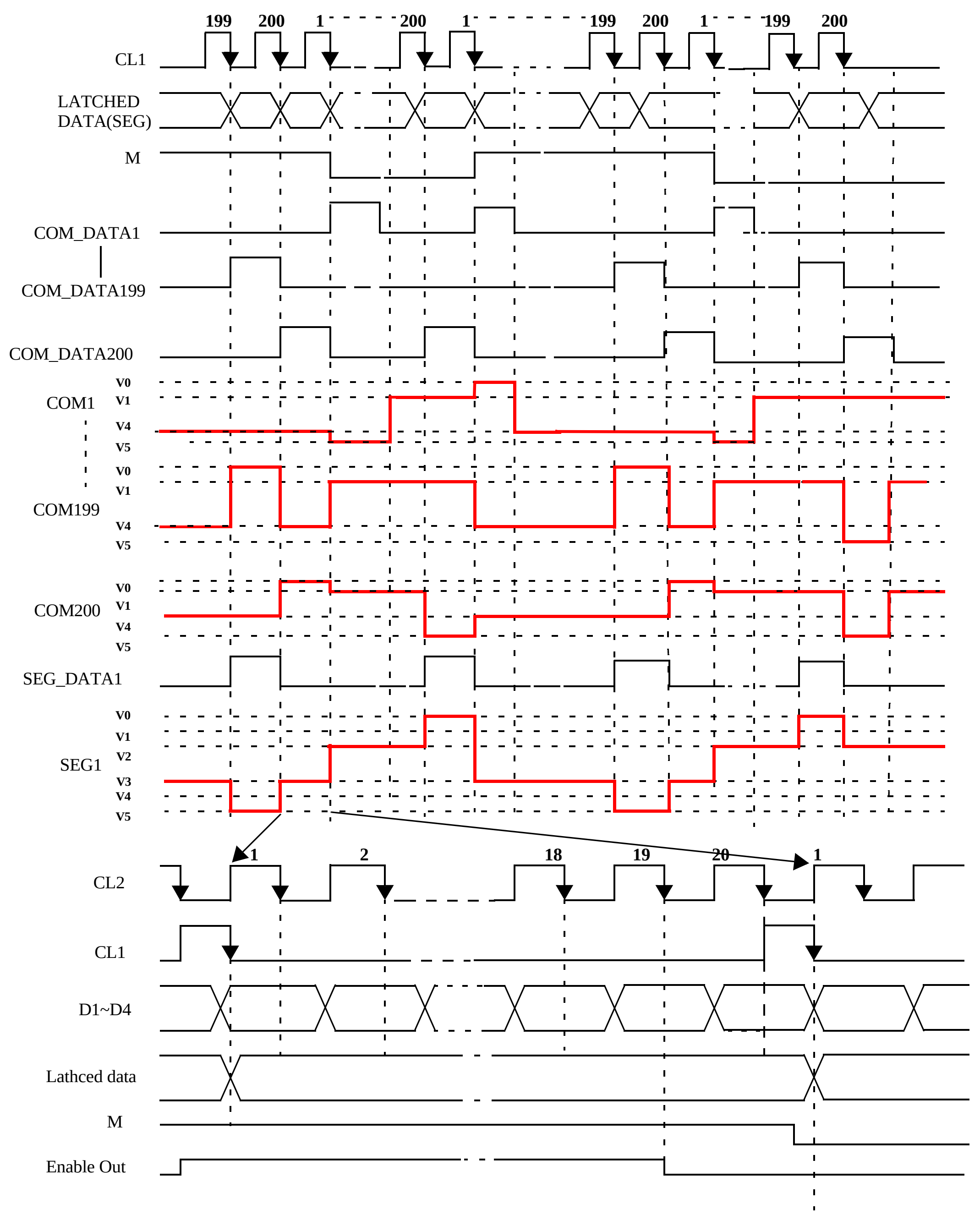


Fig.29 COMMON/SEGMENT driver timing(1/200 duty).

12 APPLICATION DIAGRAMS

12.1 4-bit parallel interface mode (80-outputs SEGMENT driver)

12.1.1 LOWER VIEW (SHL=LOW, AMS=LOW)

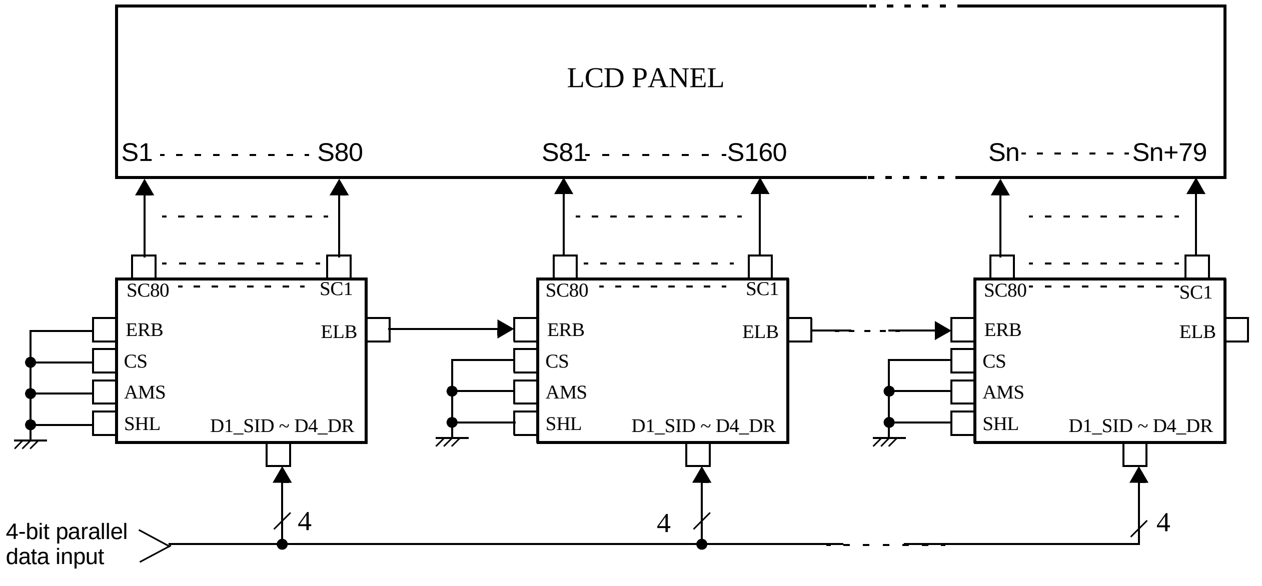


Fig.30 Lower view (SHL=LOW, AMS=LOW).

12.1.2 UPPER VIEW (SHL=HIGH, AMS=LOW)

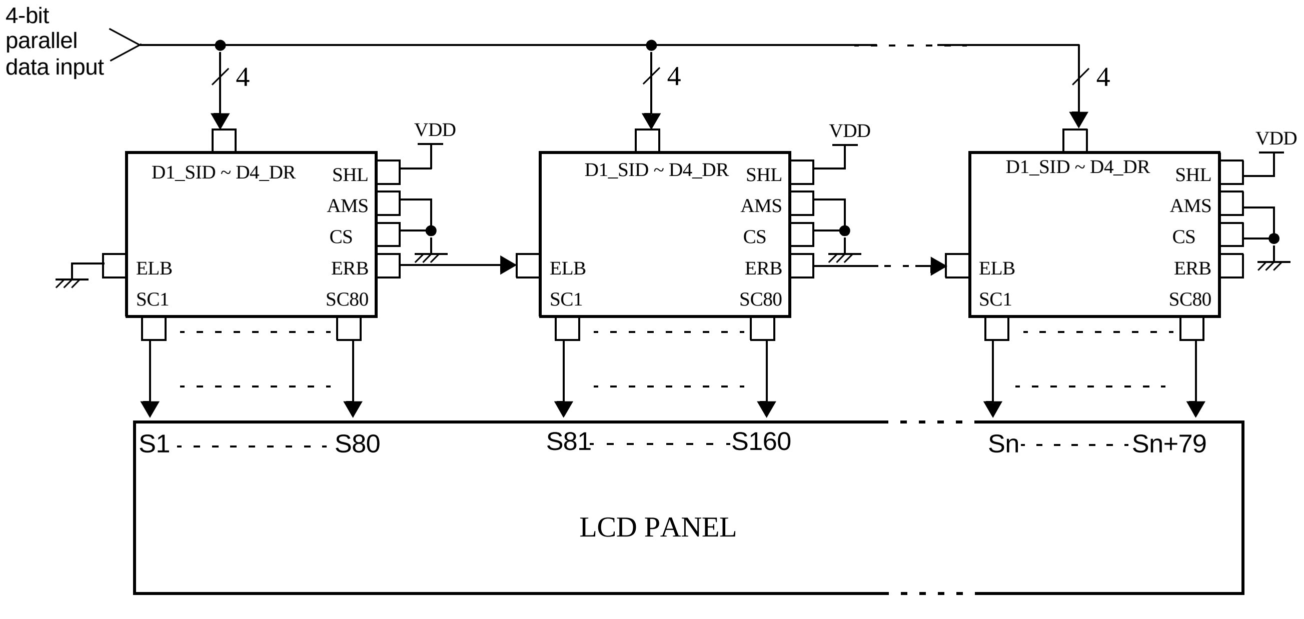


Fig.31 Upper view (SHL=HIGH, AMS=LOW).

12.2 1-bit serial interface mode (80-outputs SEGMENT driver)

12.2.1 LOWER VIEW (SHL=LOW, AMS=HIGH)

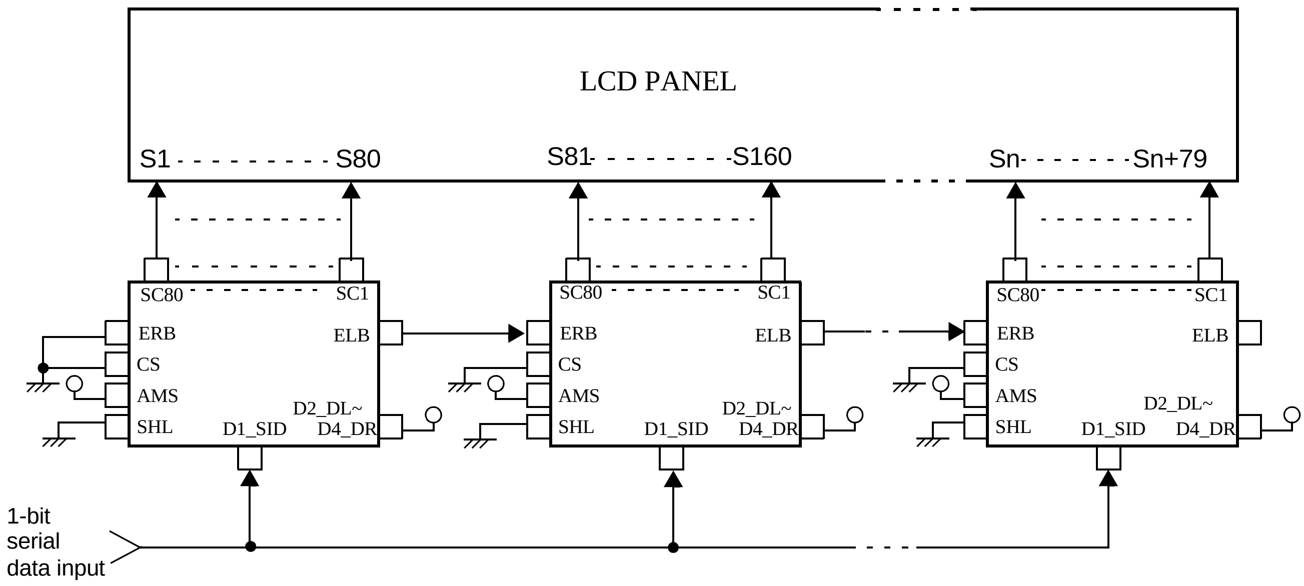


Fig.32 Lower view (SHL=L, AMS=H).

12.2.2 UPPER VIEW (SHL=HIGH, AMS=HIGH)

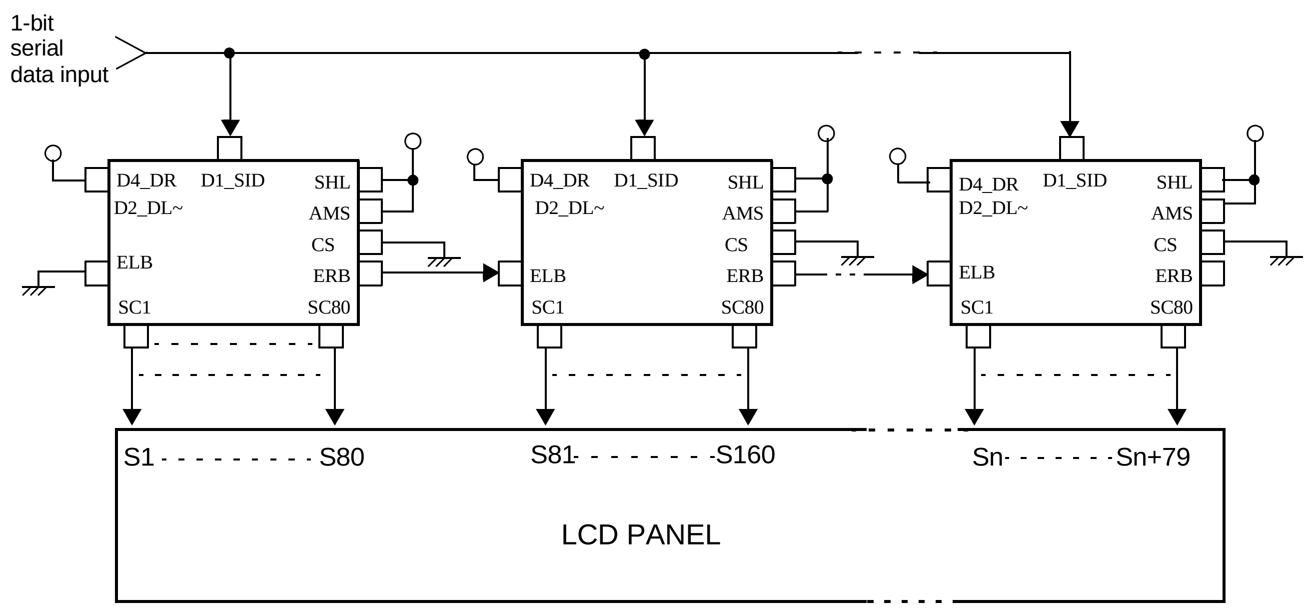


Fig.33 Upper view (SHL=HIGH, AMS=HIGH).

12.3 Single type interface mode (80-outputs COMMON driver)

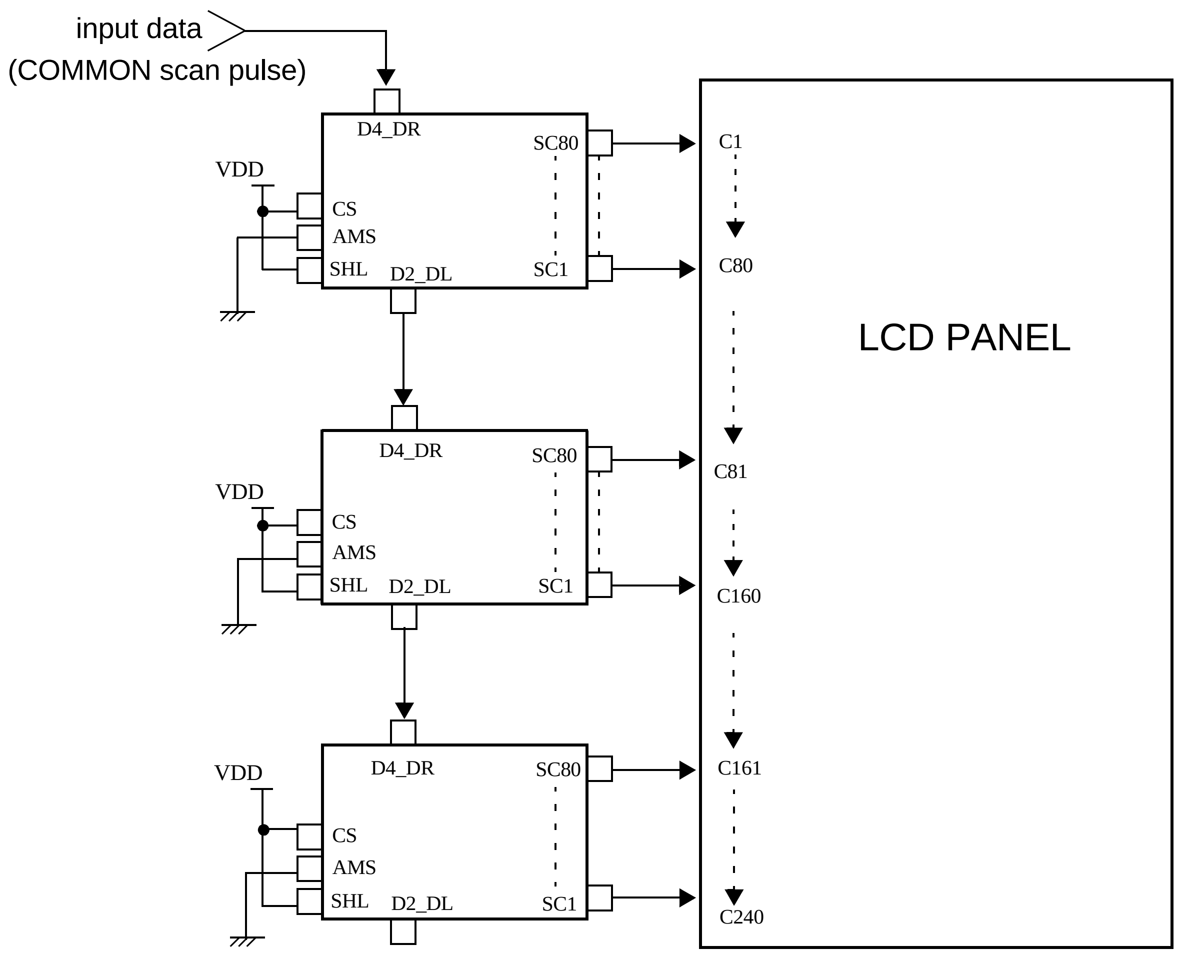
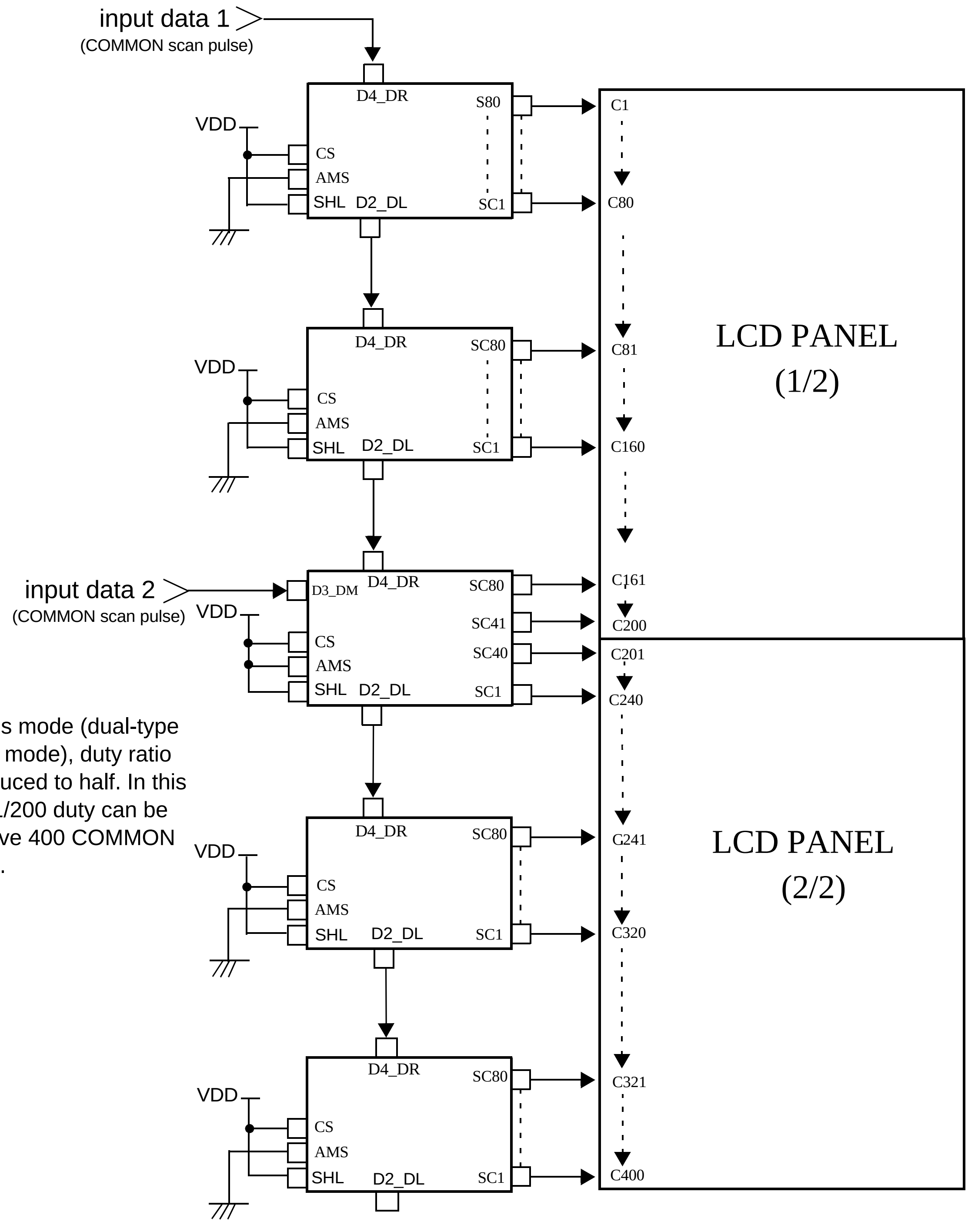


Fig.34 Single-type interface mode (80-outputs COMMON driver).

12.4 Dual type interface mode (40-outputs + 40-outputs COMMON driver)



Note: in this mode (dual-type COMMON mode), duty ratio can be reduced to half. In this example, 1/200 duty can be used to drive 400 COMMON LCD panel.

Fig.35 Dual-type interface mode (40-outputs + 40-outputs COMMON driver).

12.5 Typical application circuit

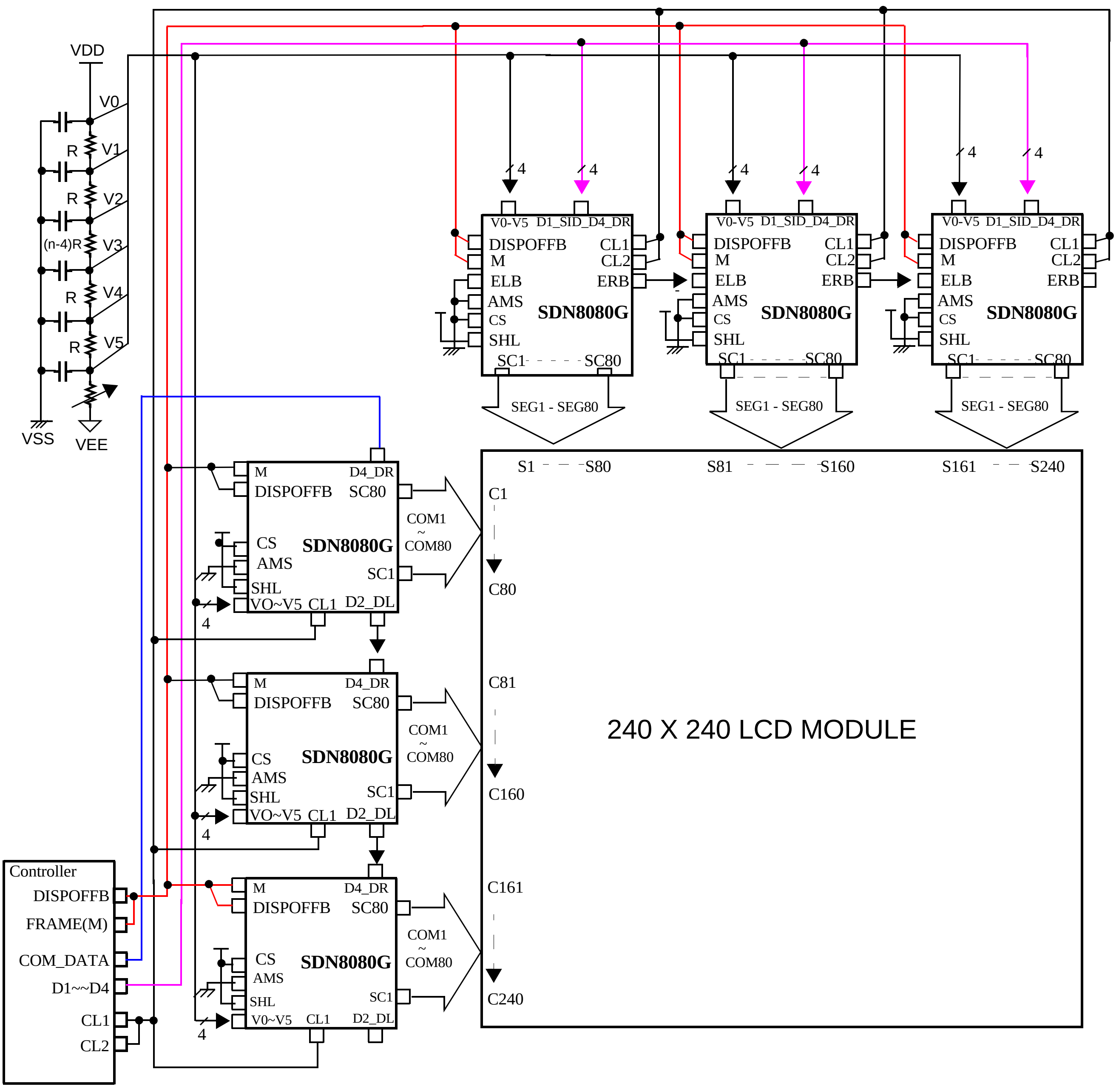
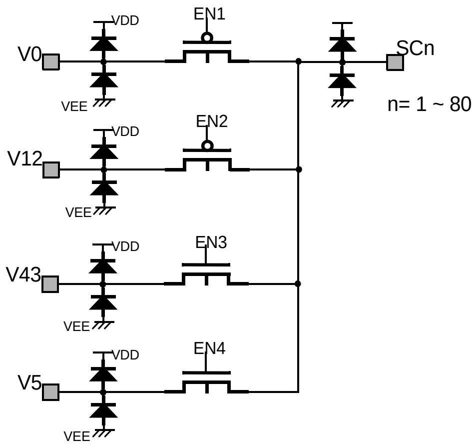
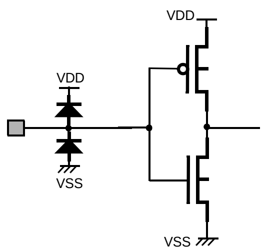
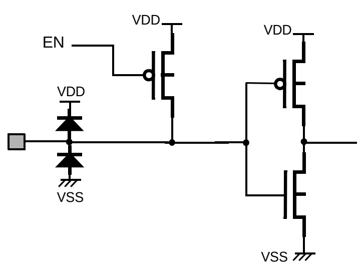
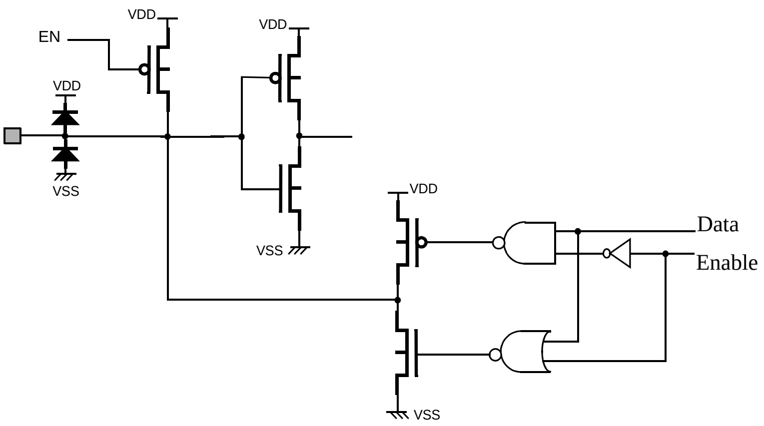
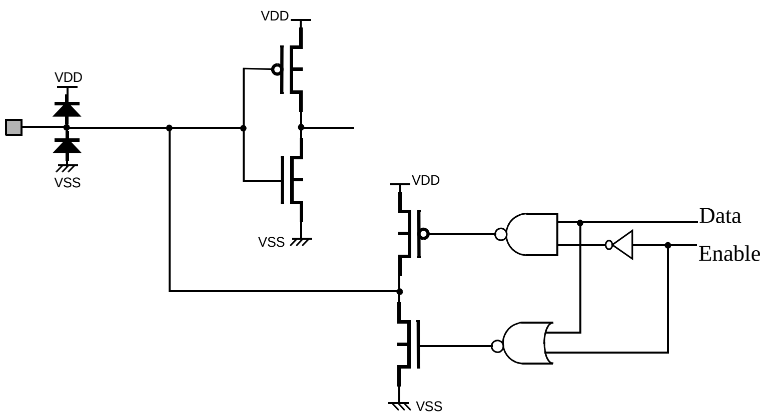


Fig.36 Typical application circuit

13 PIN CIRCUITS

Table 15 MOS-level schematics of all input, output, and I/O pins.

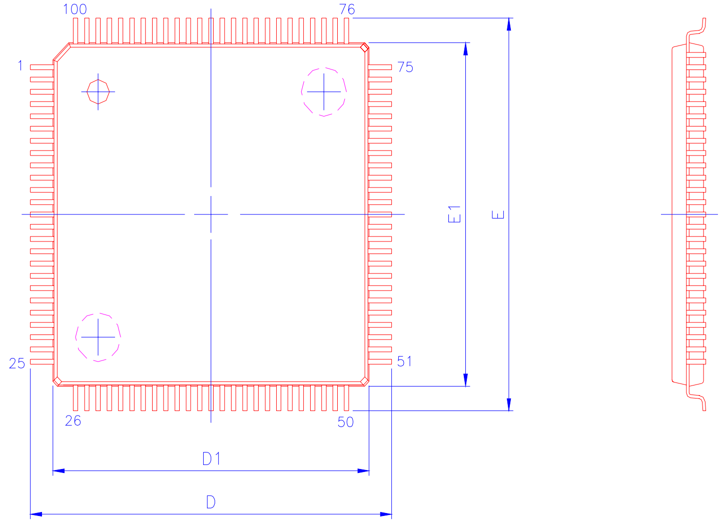
SYMBOL	Input/ output	CIRCUIT	NOTES
V0, V12, V43, V5, SC1~SC80	I/O		
CS, M, DISPOFFB, SHL, AMS, CL1	Input		
CL2, D1_SID, D3_DM	Input		

SYMBOL	Input/ output	CIRCUIT	NOTES
ELB, ERB	I/O		
D2_DL, D4_DR	I/O		

14 APPLICATION NOTES

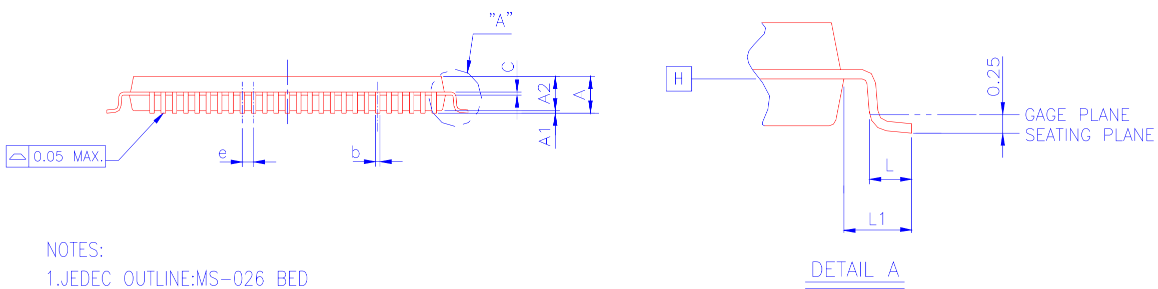
Application information is provided in another document. Please contact Avant Electronics for application information.

15 PACKAGE INFORMATION



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	0.127	0.20
D	16.00 BSC±0.25		
D1	14.00 BSC±0.1		
E	16.00 BSC±0.25		
E1	14.00 BSC±0.1		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		



NOTES:

1.JEDEC OUTLINE:MS-026 BED

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H .

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

SDN8080G
LQFP100 Package Outline Drawing

16 SOLDERING

16.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high components densities. In these situations reflow soldering is often recommended.

This text gives a very brief description to a complex technology. A more in-depth description of soldering ICs can be provided to our customers upon request.

16.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds, depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

16.3 Wave soldering

Wave soldering **is not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer, or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwelling time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.